

SHEET

TITLE

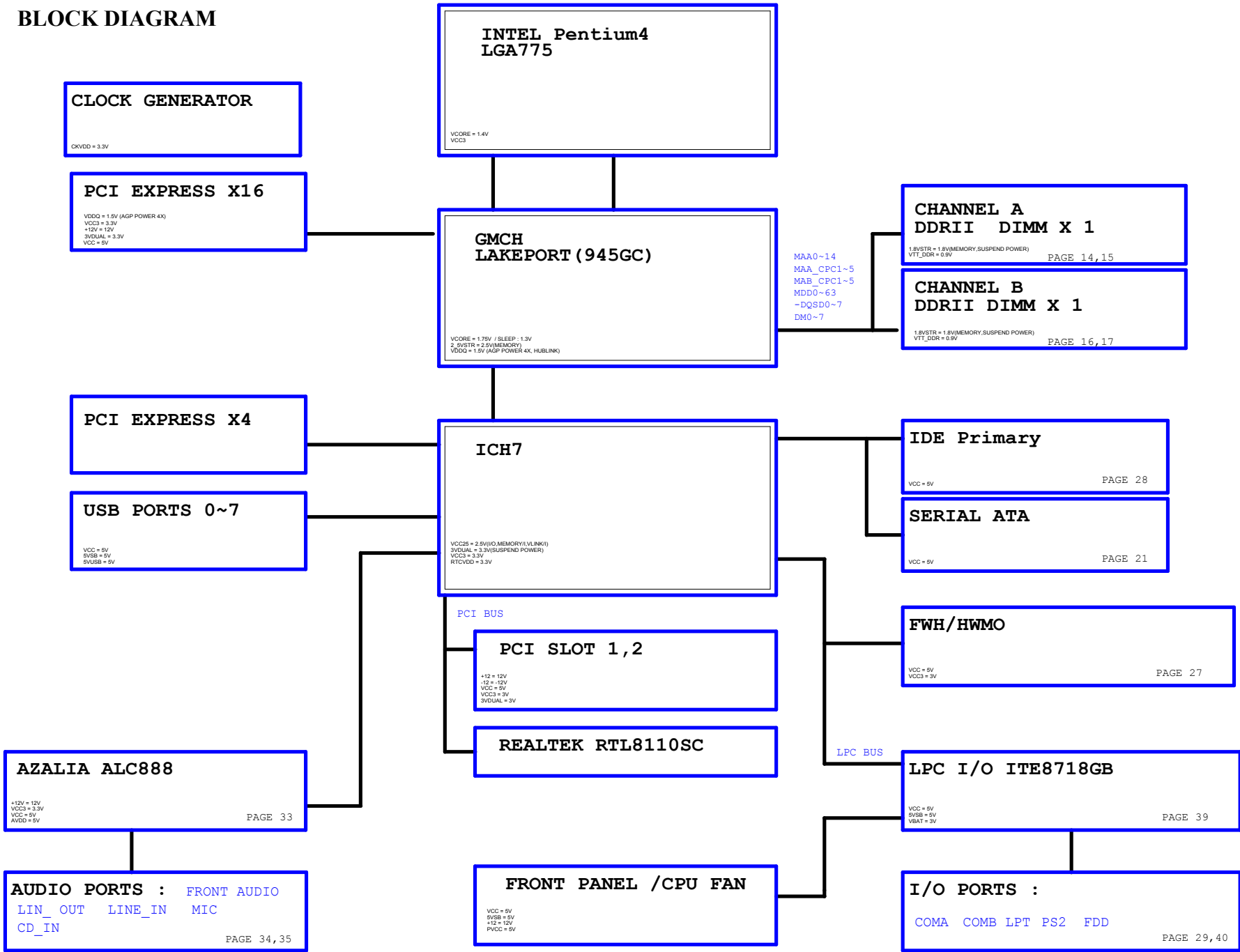
01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4 LGA775 A
05	P4 LGA775 B
06	P4 LGA775 C
07	P4 LGA775 D,E,F,G
08	GMCH-LAKEPORT HOST
09	GMCH-LAKEPORT DDRII
10	GMCH-LAKEPORT PCI E, DMI
11	GMCH-LAKEPORT INT VGA
12	GMCH-LAKEPORT GND
13	GMCH-LAKEPORT PWR
14	DDRII CHANNEL A 1
15	DDRII CHANNEL B 2
16	DDRII TERMINATION
17	PCI EXPRESS*16 SLOT
18	ICH7 PCI, USB, DMI, LAN
19	ICH7 IDE, GPIO, SATA, CTRL
20	ICH7 VCC, GND
21	GB/CK410M-OC CLOCK.
22	PCI SLOT 1,2,PCIEX4
23	IDE/FLOPPY
24	ITE 8718 GBIX
25	COM LPT
26	BIOS,CI,HWM,KB/MS
27	AZALIA ALC888

SHEET

TITLE

28	REAR AUDIO JACK
29	DISCRETE POWER
30	VCORE PWM ISL6312
31	ATX, OTHERS POWER
32	REALTEK RTL8110SC
33	FRONT PANEL

BLOCK DIAGRAM



Model Name : 945GCMX-S2

Version: 6.6

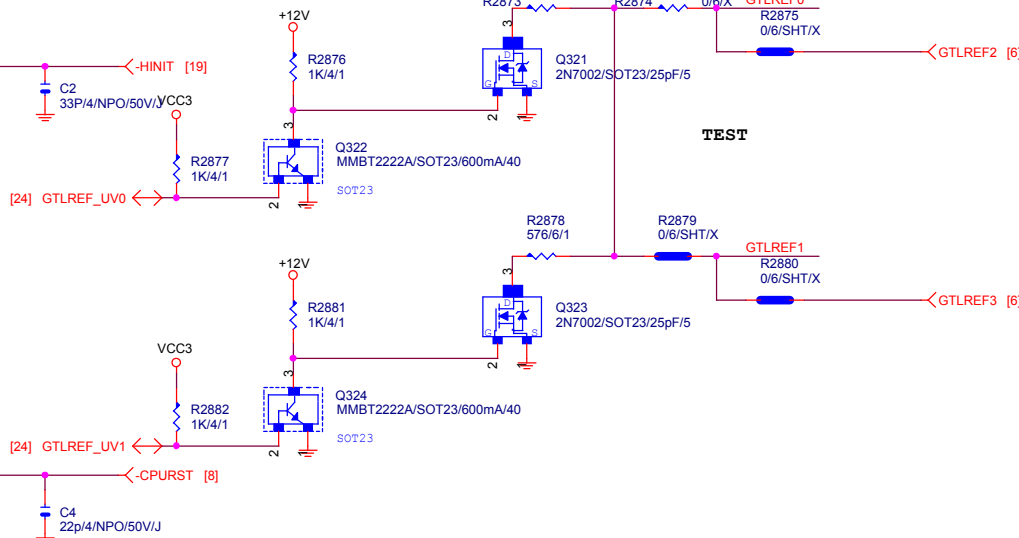
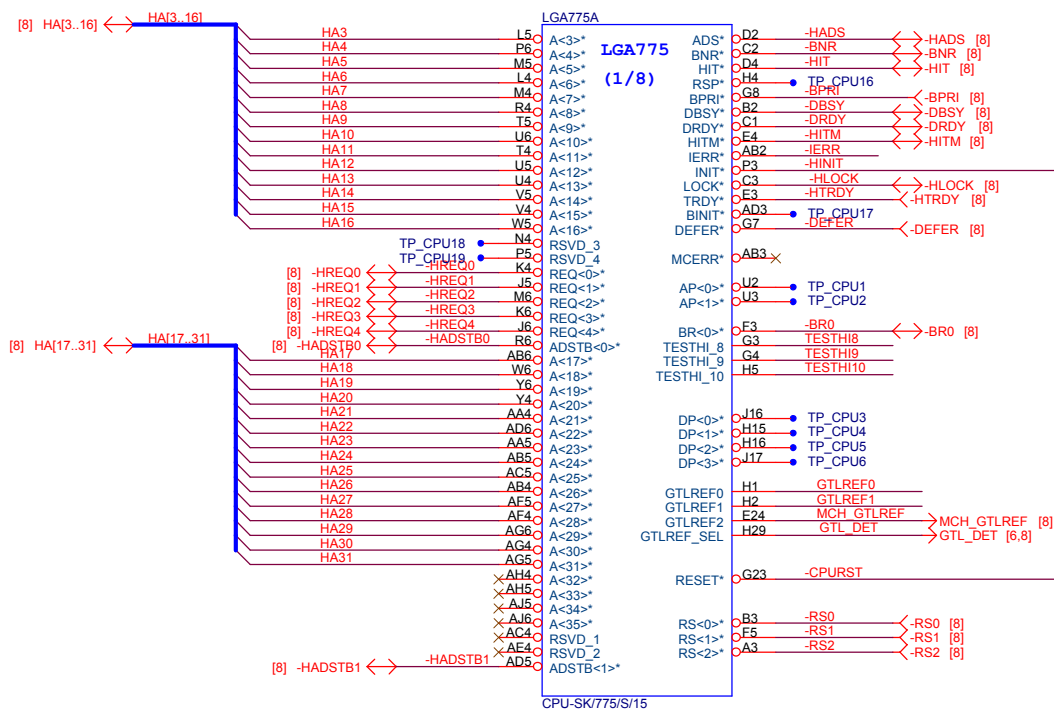
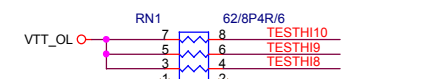
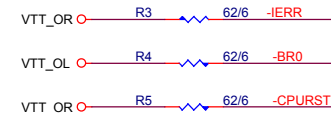
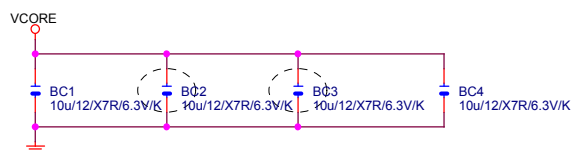
Component value change history

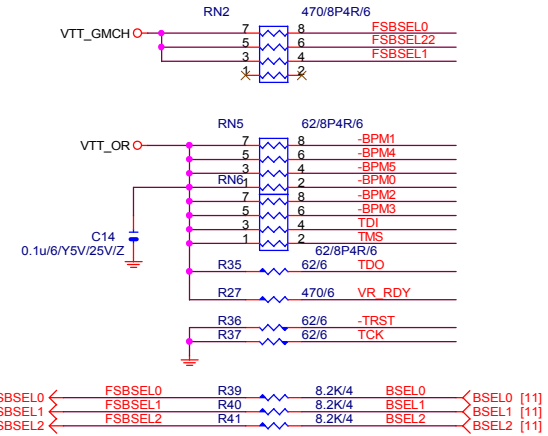
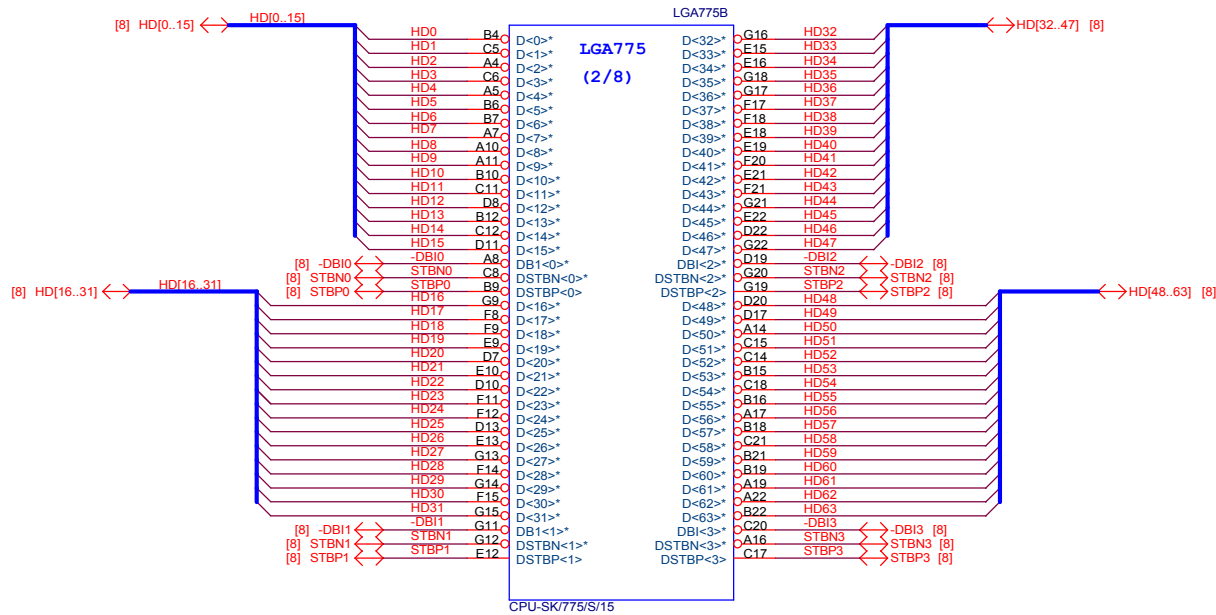
2007/03/08

[illegible]

Circuit or PCB layout change
for next version

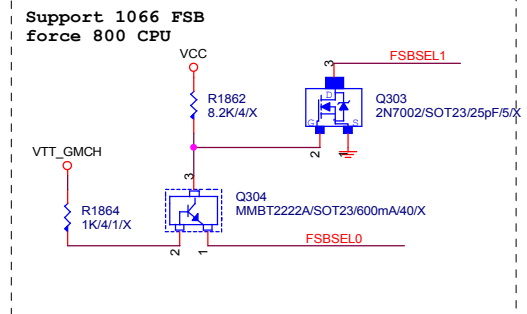
[illegible]





CPU

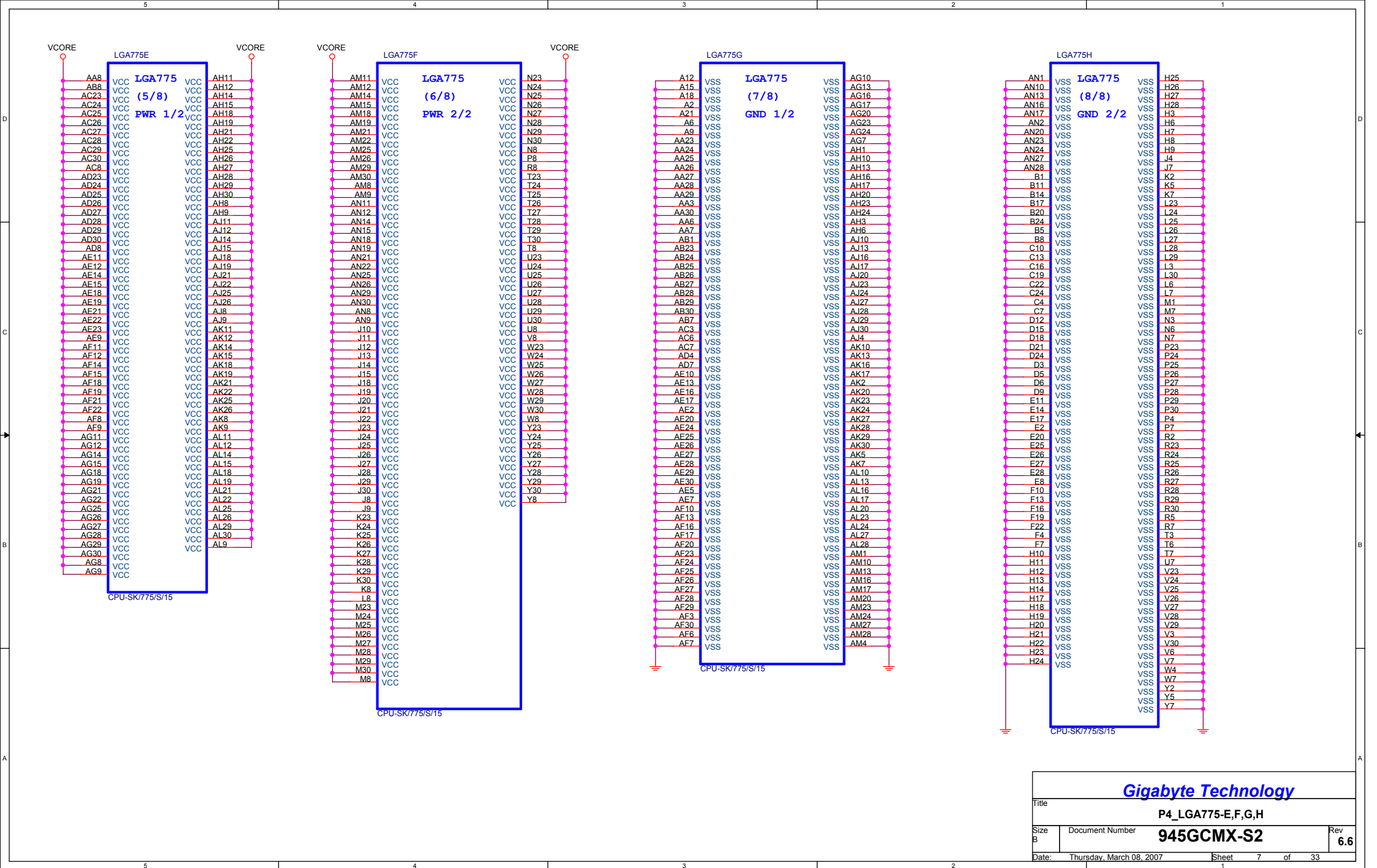
NA	FSB	FSA	
FSBSEL3	FSBSEL1	FSBSEL0	Clock
1	0	1	100MHz
0	0	1	133MHz
0	1	1	166MHz
0	1	0	200MHz
0	0	0	266MHz

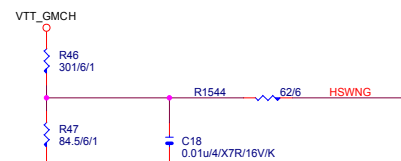
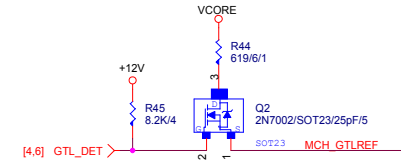
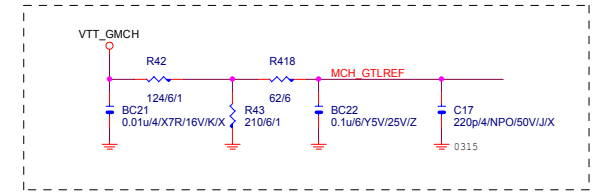
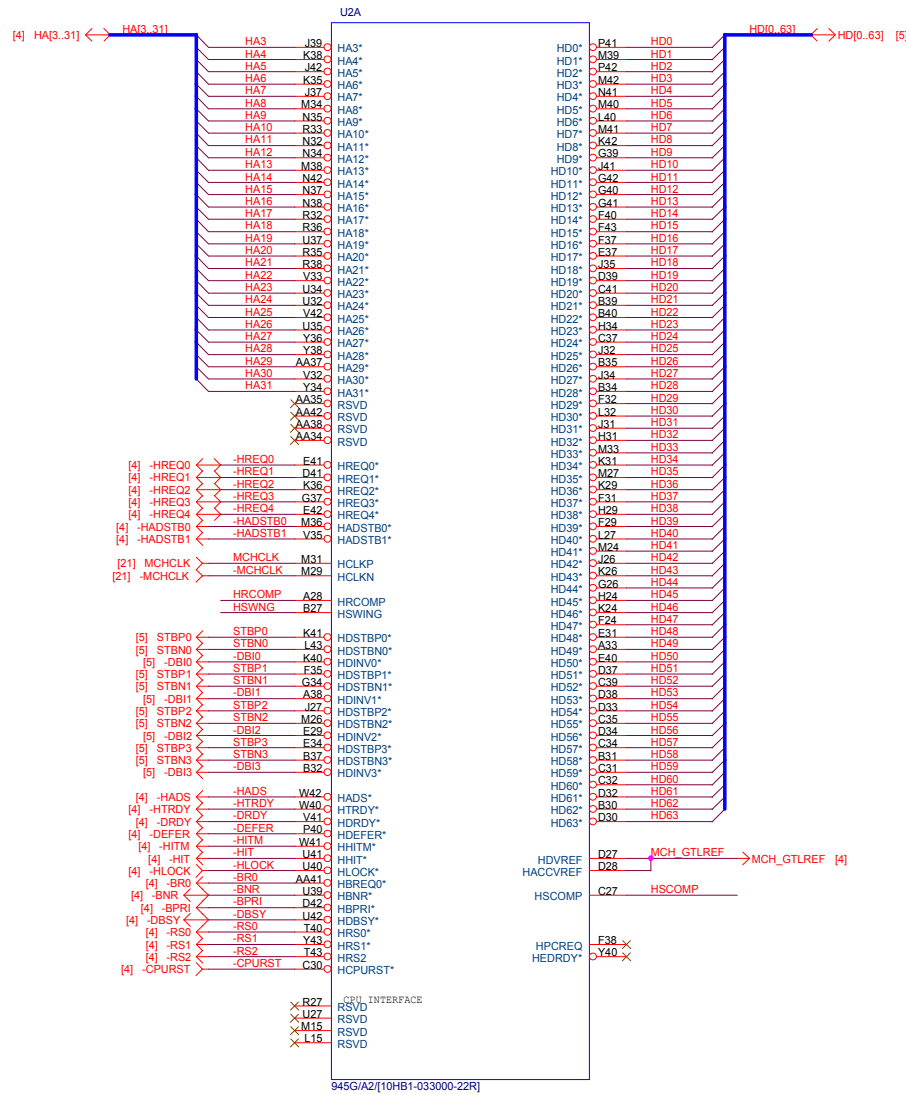


FOR FIX FSB1333 CPU

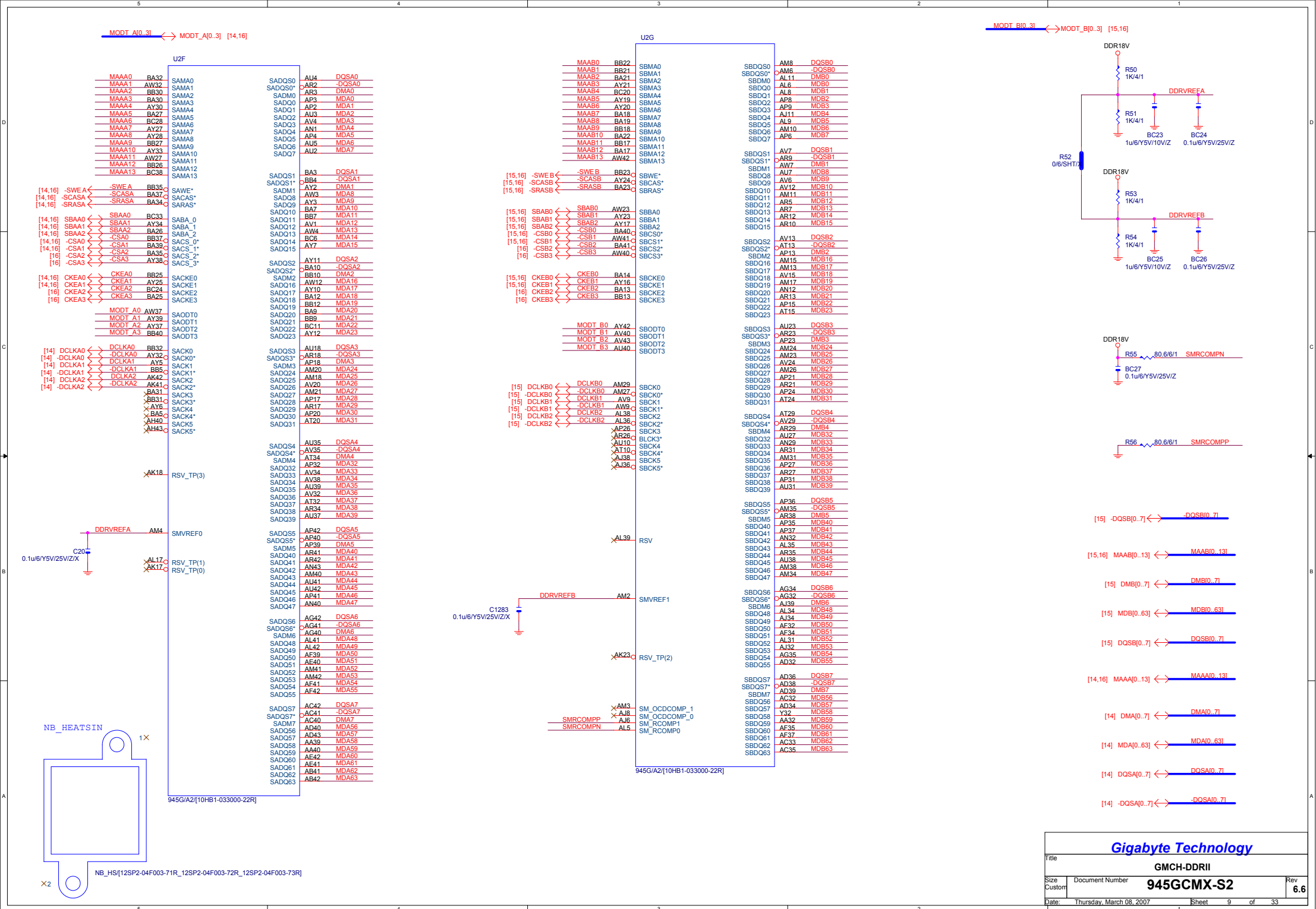
Gigabyte Technology

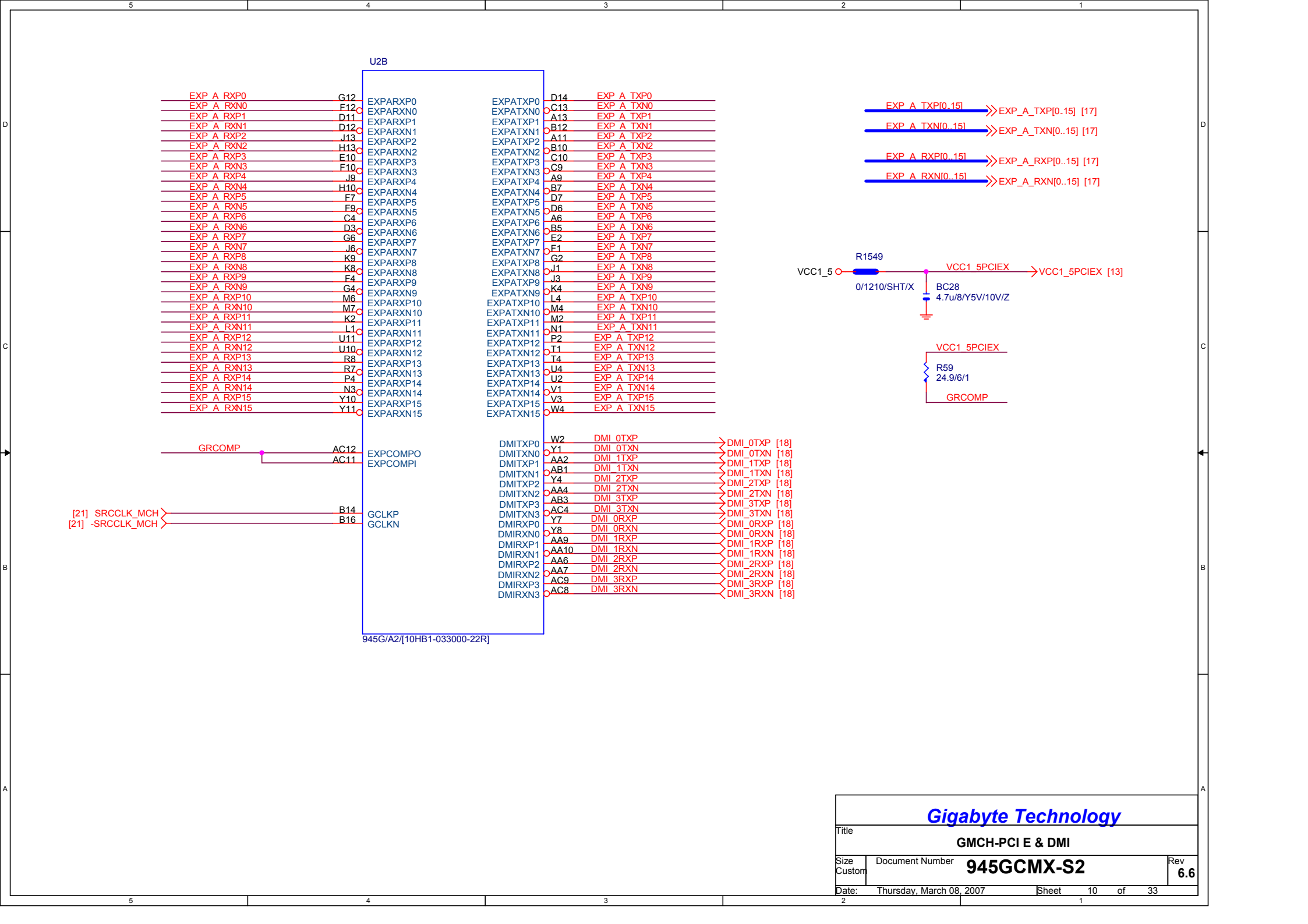
Title		P4_LGA775-B,D	
Size	Document Number	945GCMX-S2	
Custom		Rev 6.6	
Date:	Thursday, March 08, 2007	Sheet	5 of 33

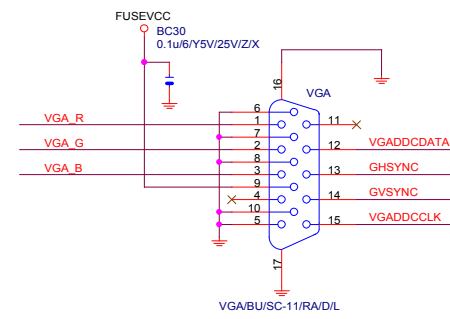
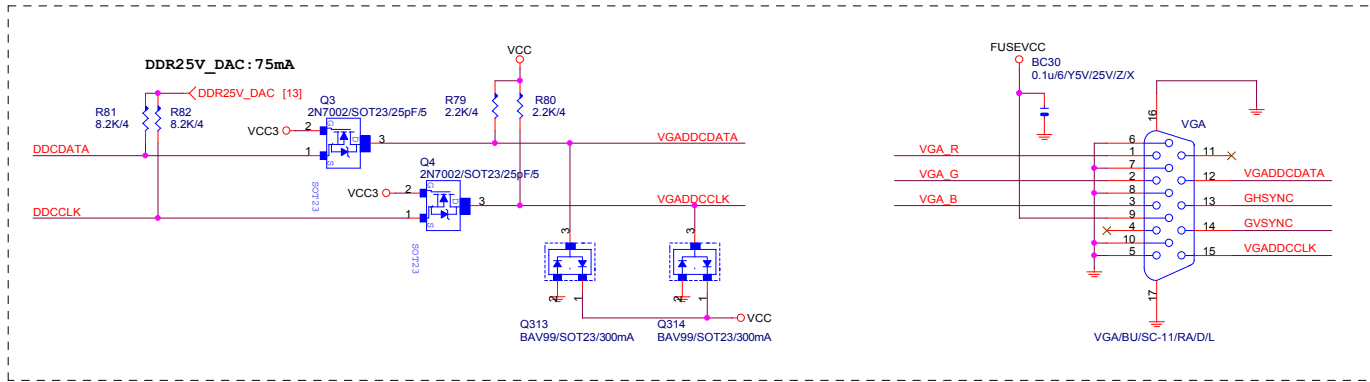
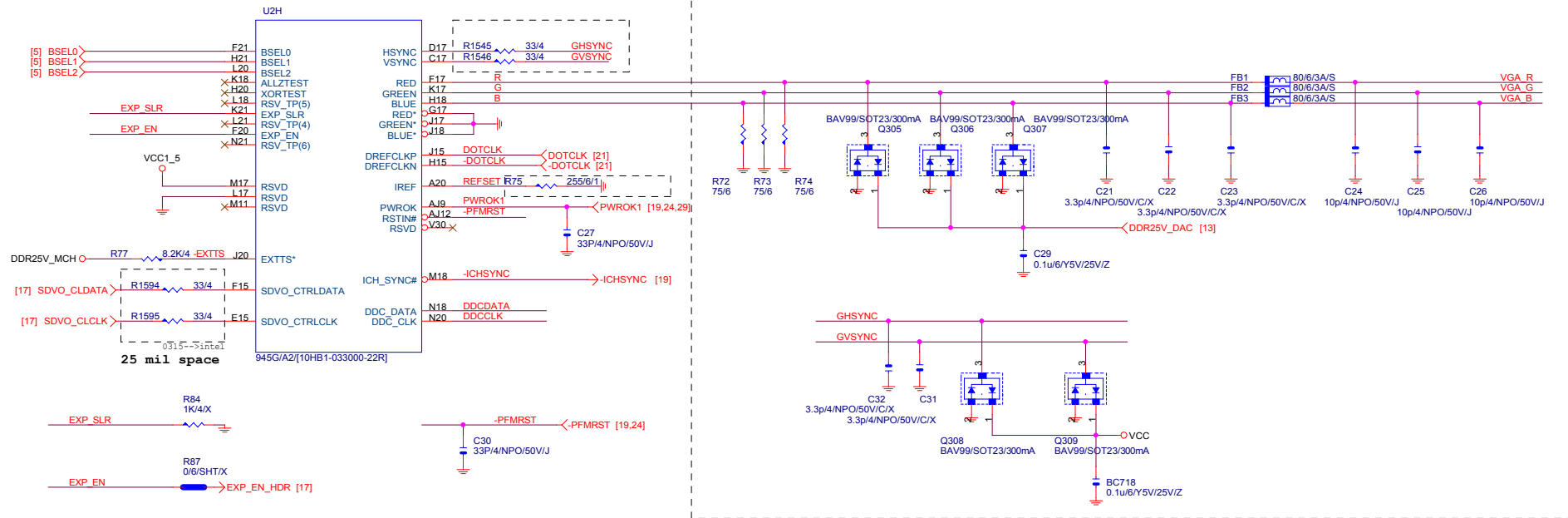


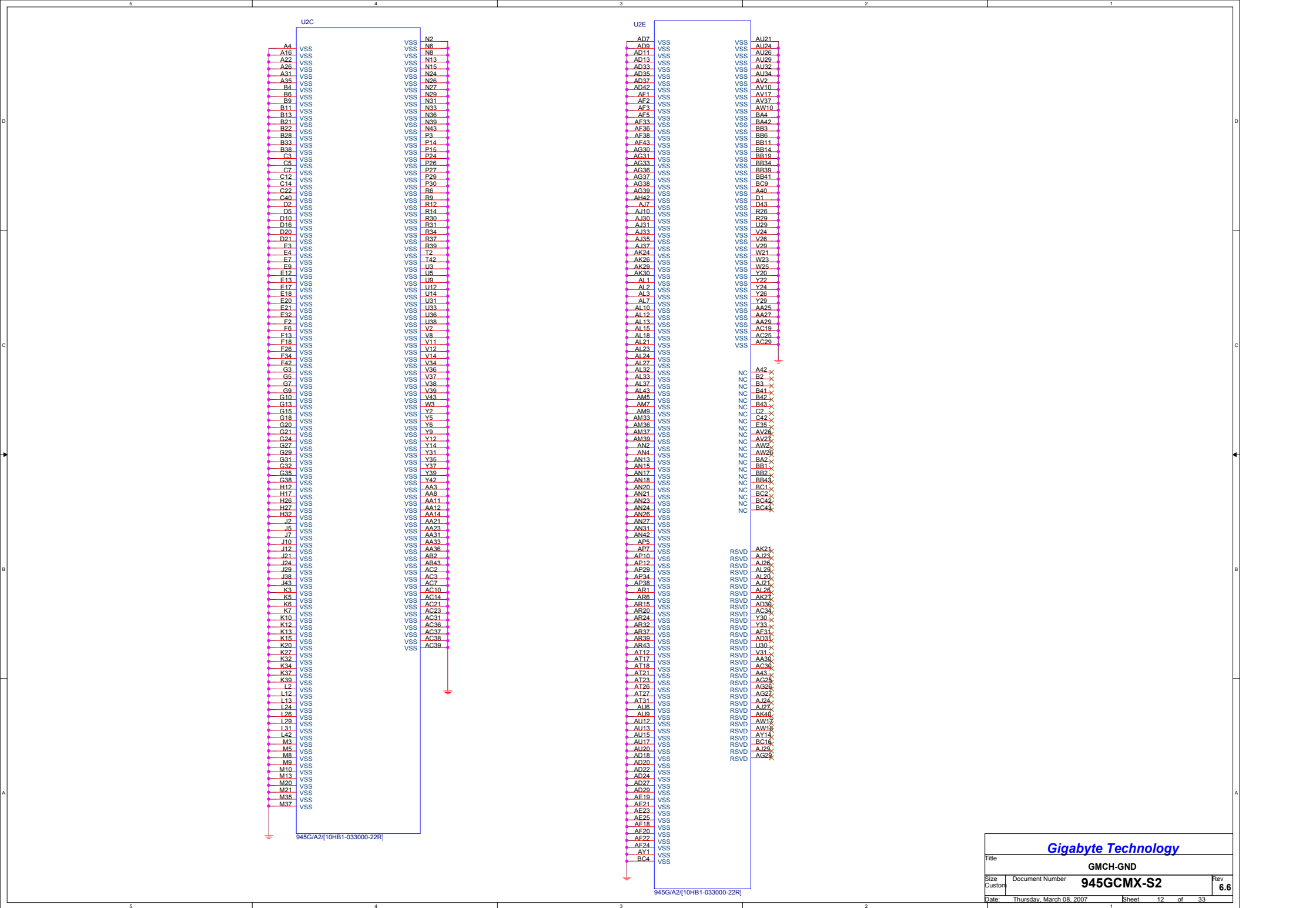


Gigabyte Technology			
Title			
GMCH-HOST			
Size	Document Number	945GCMX-S2	
Custom			Rev 6.6
Date:	Thursday, March 08, 2007	Sheet 8	of 33









1.425~1.575V

VCC1_5 0
N17 VCC
P17 VCC
P18 VCC
P20 VCC
P21 VCC
AA42 VCC
AB61 VCC
AB22 VCC
AB23 VCC
AC22 VCC
AD14 VCC
AF6 VCC
AF7 VCC
AF8 VCC
AF9 VCC
AF10 VCC
AF11 VCC
AF12 VCC
AF13 VCC
AF14 VCC
AF30 VCC
AG2 VCC
AG3 VCC
AG4 VCC
AG5 VCC
AG6 VCC
AG7 VCC
AG8 VCC
AG9 VCC
AG10 VCC
AG11 VCC
AG12 VCC
AG13 VCC
AG14 VCC
AH1 VCC
AH2 VCC
AH4 VCC
AJ5 VCC
AJ13 VCC
AJ14 VCC
AK2 VCC
AK3 VCC
AK4 VCC
AK14 VCC
AK15 VCC
AK20 VCC
R15 VCC
R17 VCC
R18 VCC
R20 VCC
R21 VCC
R23 VCC
R24 VCC
U15 VCC
U17 VCC
U18 VCC
U19 VCC
U20 VCC
U21 VCC
U22 VCC
U23 VCC
U24 VCC
U25 VCC
U26 VCC
V15 VCC
V17 VCC
V18 VCC
V19 VCC
V20 VCC
V21 VCC
V22 VCC
V23 VCC
V24 VCC
V25 VCC
W7 VCC
W17 VCC
W18 VCC
W19 VCC
W20 VCC
W22 VCC
W24 VCC
W26 VCC
W27 VCC
Y15 VCC
Y17 VCC
Y18 VCC
Y19 VCC
Y21 VCC
Y23 VCC
Y25 VCC
Y27 VCC
AA15 VCC
AA17 VCC
AA18 VCC
AA19 VCC
AA20 VCC
AA24 VCC
AA26 VCC
AB17 VCC
AB18 VCC
AB19 VCC
AB20 VCC
AB24 VCC
AB25 VCC
AB26 VCC
AB27 VCC
AC15 VCC
AC17 VCC
AC18 VCC
AC20 VCC
AC24 VCC
AC26 VCC
AC27 VCC
AD15 VCC
AD17 VCC
AD19 VCC
AD21 VCC
AD23 VCC
AD25 VCC
AD26 VCC
AE17 VCC
AE18 VCC
AE20 VCC
AE22 VCC
AE24 VCC
AE26 VCC
AE27 VCC
AE15 VCC
AE17 VCC
AE19 VCC
AE21 VCC
AE23 VCC
AE25 VCC
AE26 VCC
AE27 VCC
AE29 VCC

945G/A2[10HBT-033000-22R]

1.7~1.9V

DDR18V

VCCSM BB16
VCCSM AW15
VCCSM BB42
VCCSM BC11
VCCSM BC18
VCCSM BC22
VCCSM BC26
VCCSM BB20
VCCSM AW24
VCCSM BC35
VCCSM BC31
VCCSM BB38
VCCSM BB33
VCCSM BB28
VCCSM BB24
VCCSM AW29
VCCSM AW31
VCCSM AW34
VCCSM AW41
VCCSM AW42
VCCSM AW23
VCCSM AW18
VCCSM BC40
VCCSM AW35
VCCSM AW43
VCCSM AW20
VCCSM AW21
VCCSM AW13
VCCSM AW21

1.14~1.26V

VTT_GMCH

VTT C23
VTT G23
VTT P23
VTT E23
VTT D23
VTT D24
VTT D25
VTT B25
VTT B24
VTT B23
VTT B26
VTT H23
VTT J23
VTT K23
VTT L23
VTT M23
VTT E24
VTT N23
VTT A24
VTT F27
VTT E27
VTT E26
VTT C25
VTT C26

VCCA_DPLL B19
VCCA_MPLL B20
VCCA_HPLL C21
VCCA_DPLLA C19
VCCA_DPLLB B18
VCCA_DAC C18
VCCA_EXPPLL V22
VCCA_EXPPLL V21
VCCA_EXPPLL V23
VCCA_EXPPLL V25
VCCA_EXPPLL W17
VCCA_EXPPLL W18
VCCA_EXPPLL W19
VCCA_EXPPLL W20
VCCA_EXPPLL W22
VCCA_EXPPLL W24
VCCA_EXPPLL W26
VCCA_EXPPLL W27
VCCA_EXPPLL Y15
VCCA_EXPPLL Y17
VCCA_EXPPLL Y18
VCCA_EXPPLL Y19
VCCA_EXPPLL Y21
VCCA_EXPPLL Y23
VCCA_EXPPLL Y25
VCCA_EXPPLL Y27
VCCA_EXPPLL AA15
VCCA_EXPPLL AA17
VCCA_EXPPLL AA18
VCCA_EXPPLL AA19
VCCA_EXPPLL AA20
VCCA_EXPPLL AA24
VCCA_EXPPLL AA26
VCCA_EXPPLL AB17
VCCA_EXPPLL AB18
VCCA_EXPPLL AB19
VCCA_EXPPLL AB20
VCCA_EXPPLL AB24
VCCA_EXPPLL AB25
VCCA_EXPPLL AB26
VCCA_EXPPLL AB27
VCCA_EXPPLL AC15
VCCA_EXPPLL AC17
VCCA_EXPPLL AC18
VCCA_EXPPLL AC20
VCCA_EXPPLL AC24
VCCA_EXPPLL AC26
VCCA_EXPPLL AC27
VCCA_EXPPLL AD15
VCCA_EXPPLL AD17
VCCA_EXPPLL AD19
VCCA_EXPPLL AD21
VCCA_EXPPLL AD23
VCCA_EXPPLL AD25
VCCA_EXPPLL AD26
VCCA_EXPPLL AE17
VCCA_EXPPLL AE18
VCCA_EXPPLL AE20
VCCA_EXPPLL AE22
VCCA_EXPPLL AE24
VCCA_EXPPLL AE26
VCCA_EXPPLL AE27
VCCA_EXPPLL AE15
VCCA_EXPPLL AE17
VCCA_EXPPLL AE19
VCCA_EXPPLL AE21
VCCA_EXPPLL AE23
VCCA_EXPPLL AE25
VCCA_EXPPLL AE26
VCCA_EXPPLL AE27
VCCA_EXPPLL AE29

2.375~2.625V

VCCA_DAC=DDR25V_DAC=70mA (2.375~2.625V)

DDR25V_MCH FB4

DDR25V_DAC [11]

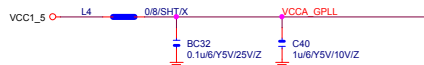
VCCA_5PCIE_X [10]

1.425~1.575V

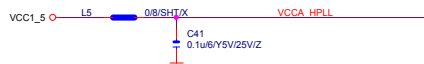
VCC EXP AA13
VCC EXP AD12
VCC EXP AC5
VCC EXP AA5
VCC EXP V5
VCC EXP V13
VCC EXP AE2
VCC EXP R13
VCC EXP N12
VCC EXP N10
VCC EXP R6
VCC EXP N7
VCC EXP N11
VCC EXP AE3
VCC EXP N9
VCC EXP AD10
VCC EXP AD1
VCC EXP AC6
VCC EXP AD8
VCC EXP AD2
VCC EXP AD4
VCC EXP AD5
VCC EXP AD6
VCC EXP Y13
VCC EXP N6
VCC EXP U8
VCC EXP AC13
VCC EXP AE4
VCC EXP U7
VCC EXP R10
VCC EXP U6
VCC EXP V6
VCC EXP V7
VCC EXP V9
VCC EXP V10

VCC AG15
VCC AG17
VCC AG18
VCC AG19
VCC AG20
VCC AG21
VCC AG22
VCC AG23
VCC AG24
VCC AJ15
VCC AJ17
VCC AJ18
VCC AJ20

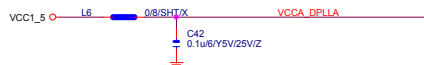
VCCA_EXPPLL=VCCA_GPLL=45mA (1.425V~1.575V)



VCCA_HPLL>50mA 公板爲200mA (1.425V~1.575V)



VCCA_DPLLA=65mA (1.425V~1.575V)



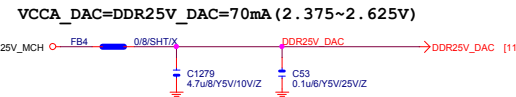
VCCA_DPLLB=65mA (1.425V~1.575V)



VCCA_MPLL>50mA (1.425V~1.575V)



VCCA_DAC=DDR25V_DAC=70mA (2.375~2.625V)



945 Design Guide rev1.5 spec.

VCCA_EXPPLL=VCCA_GPLL=45mA (1.425V~1.575V)

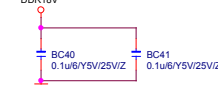
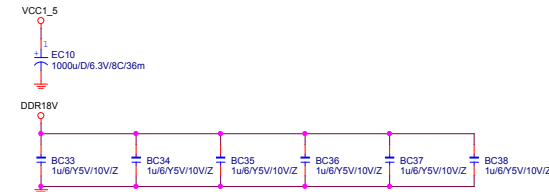
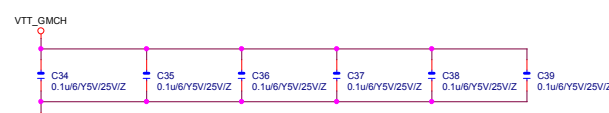
VCCA_HPLL>50mA 公板爲200mA (1.425V~1.575V)

VCCA_DPLLA=65mA (1.425V~1.575V)

VCCA_DPLLB=65mA (1.425V~1.575V)

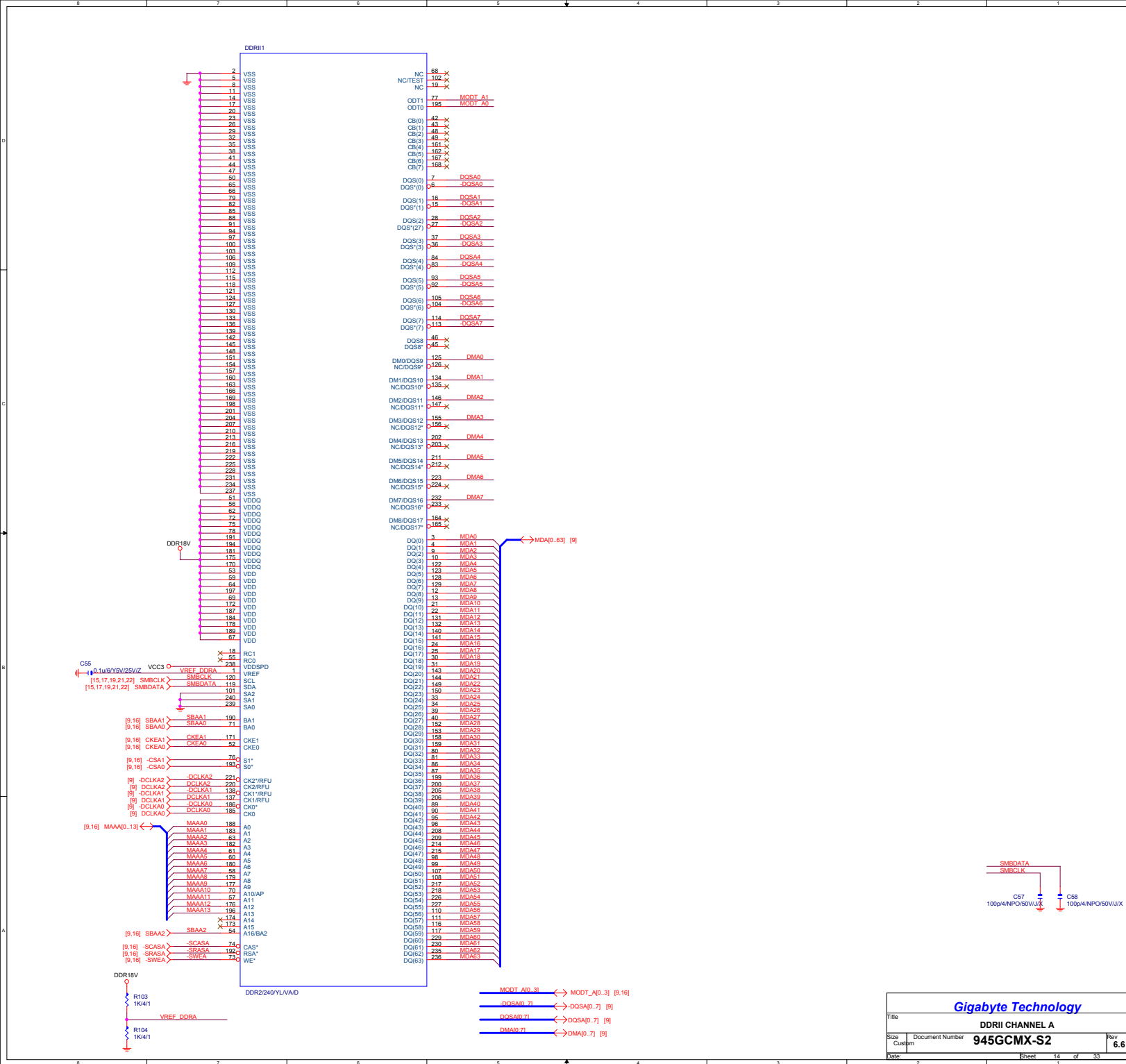
VCCA_MPLL>50mA (1.425V~1.575V)

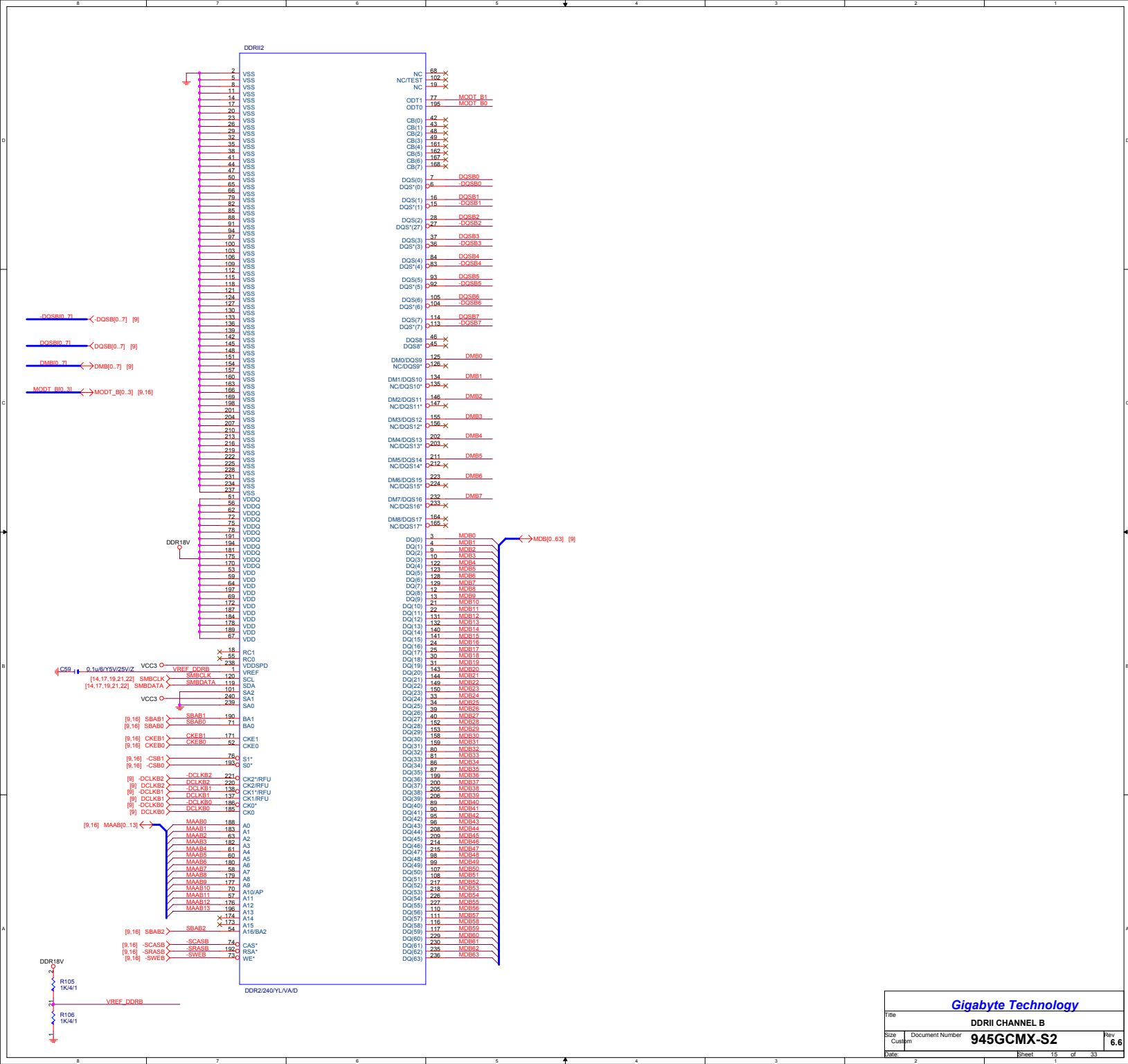
VCCA_DAC=DDR25V_DAC=70mA (2.375~2.625V)



Gigabyte Technology

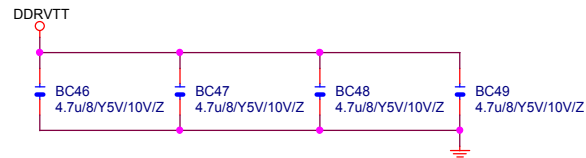
File	GMCH-PWR	
Size	Document Number	945GCMX-S2
Custom		Rev 6.6
Date	Thursday, March 08, 2007	Sheet 13 of 33





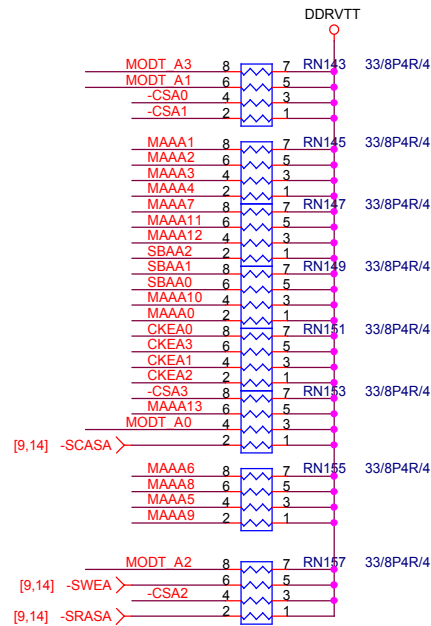
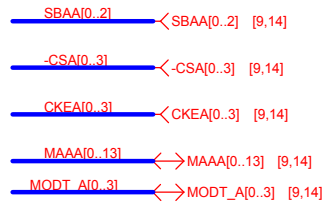
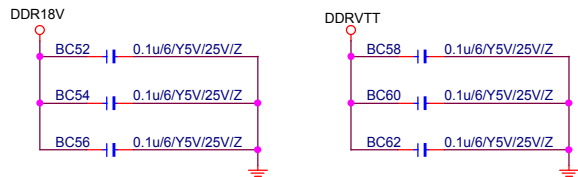
DDR TERMINATION CHANNEL A

DDRVTT Decouple



DDR18V Decouple

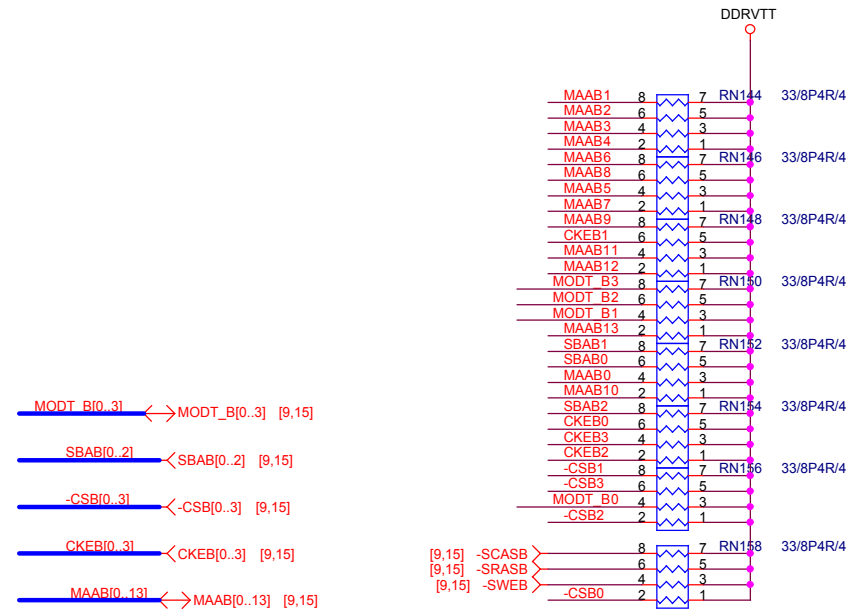
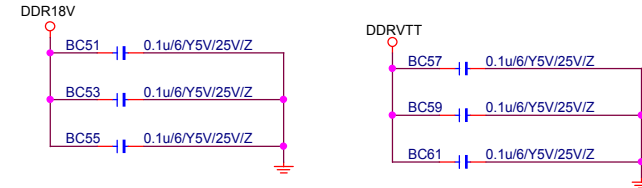
DDRVTT Decouple

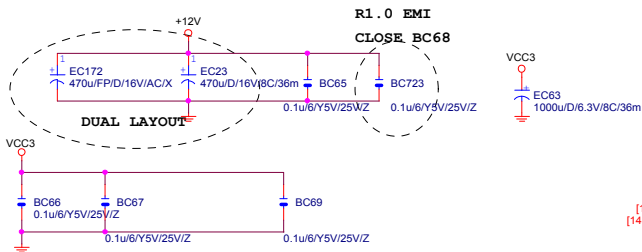


DDR TERMINATION CHANNEL B

DDR18V Decouple

DDRVTT Decouple

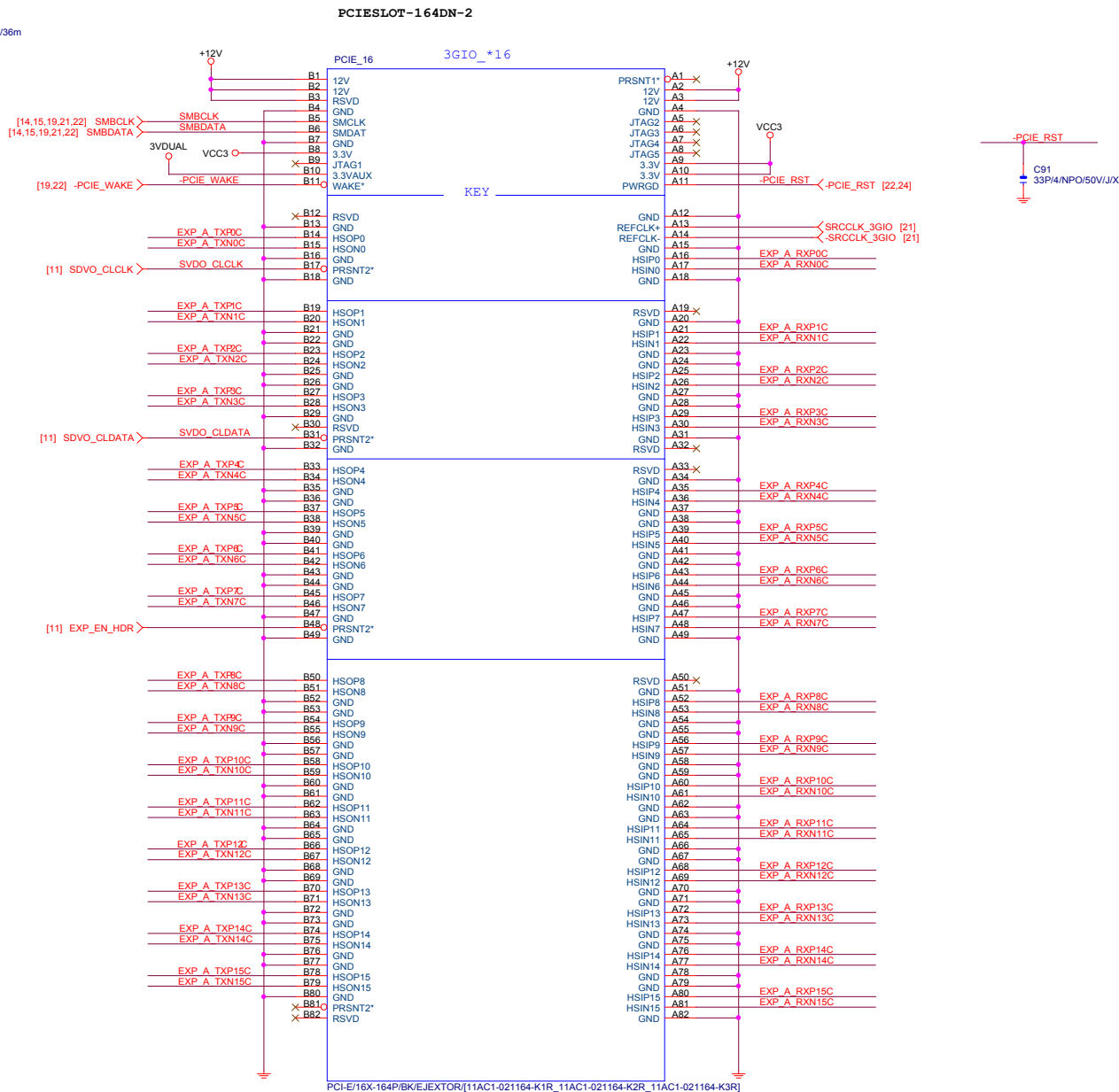


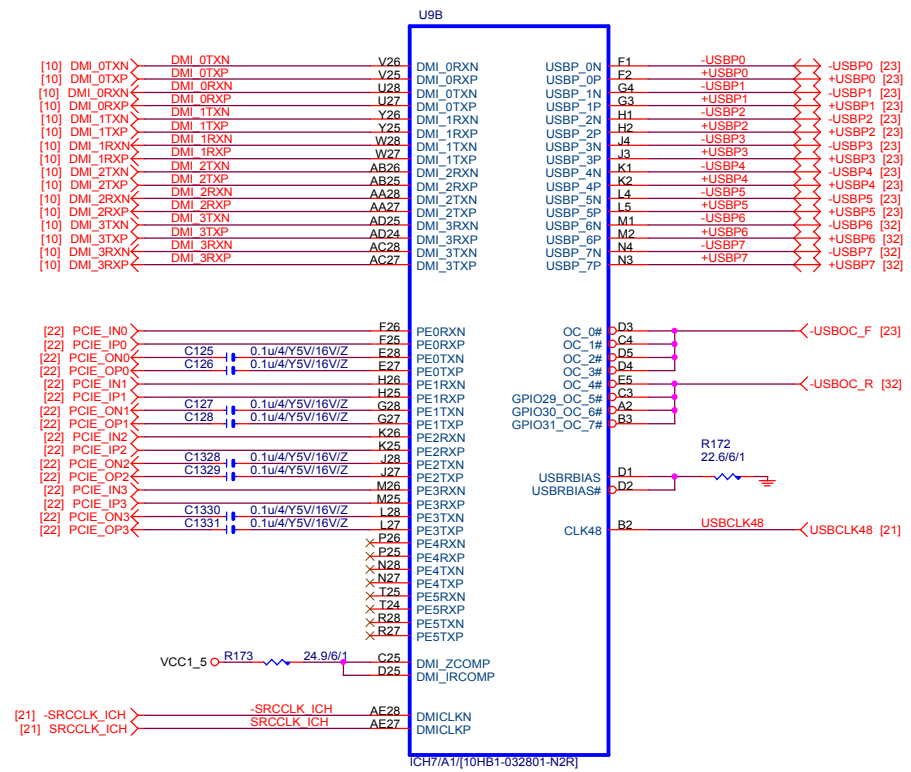
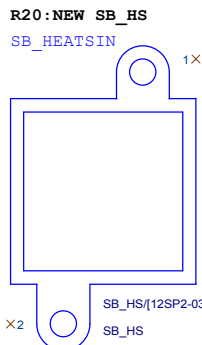
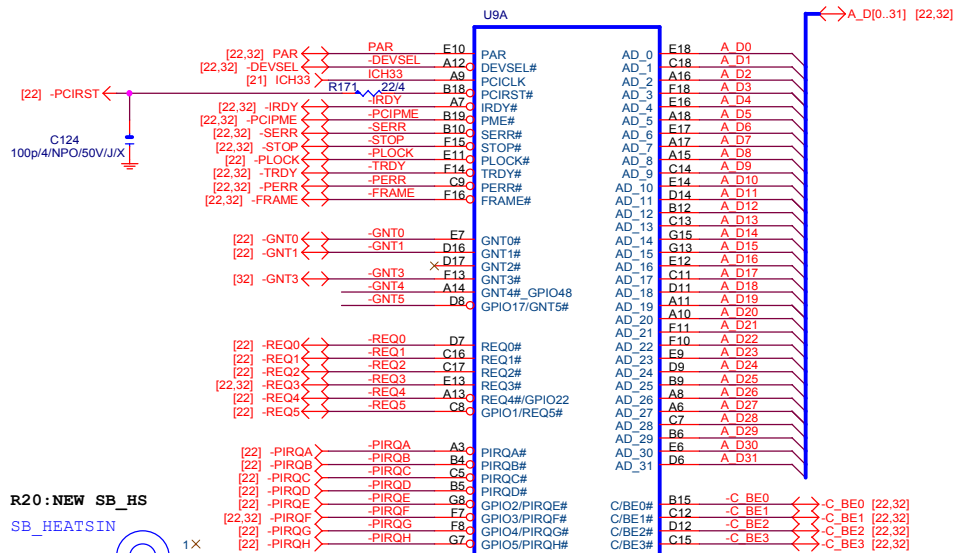


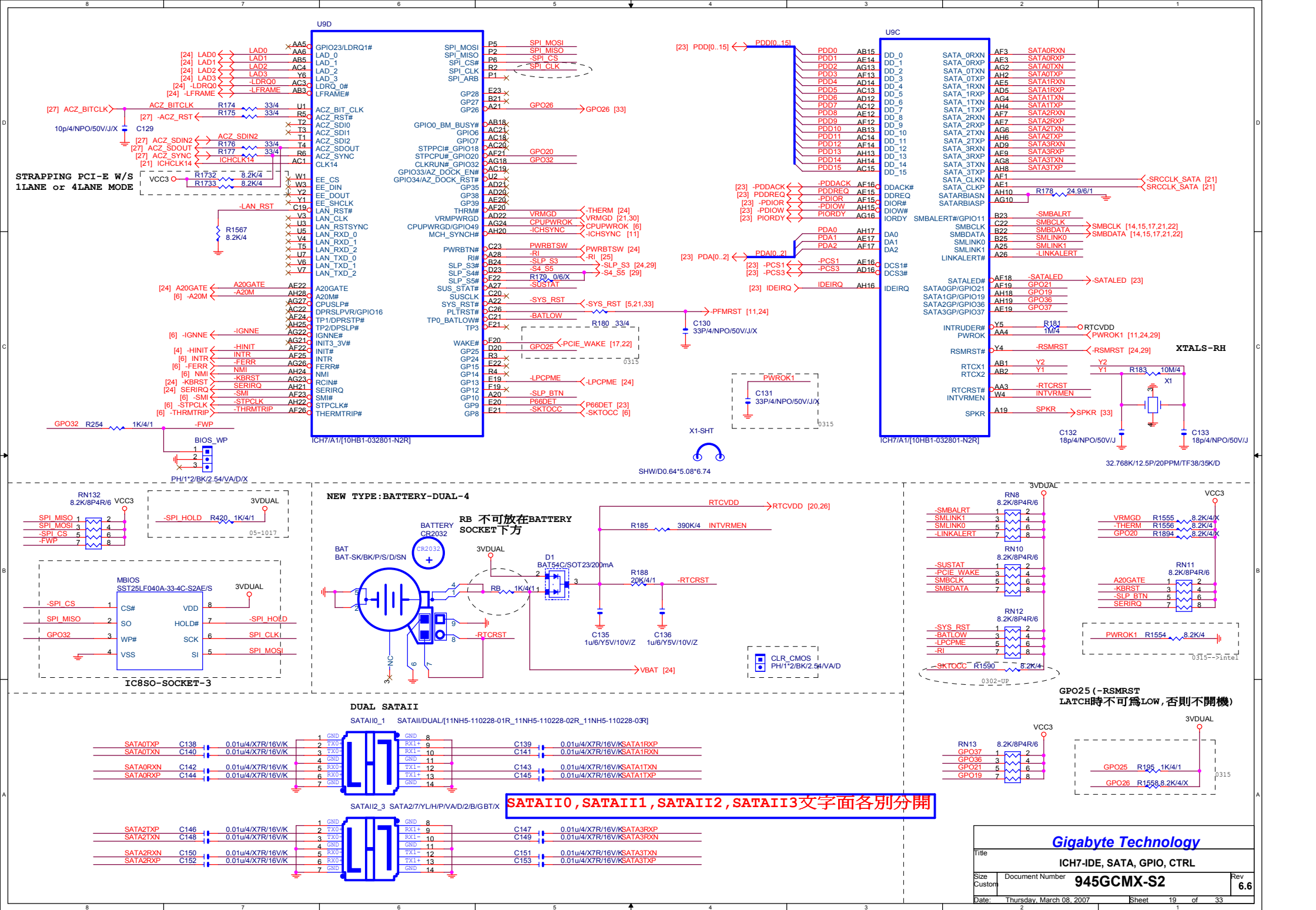
EXP A TXP0_15] >> EXP_A_TXP0_15] [10] EXP A RXP0_15] >> EXP_A_RXP0_15] [10]
EXP A TXN0_15] >> EXP_A_TXN0_15] [10] EXP A RXN0_15] >> EXP_A_RXN0_15] [10]

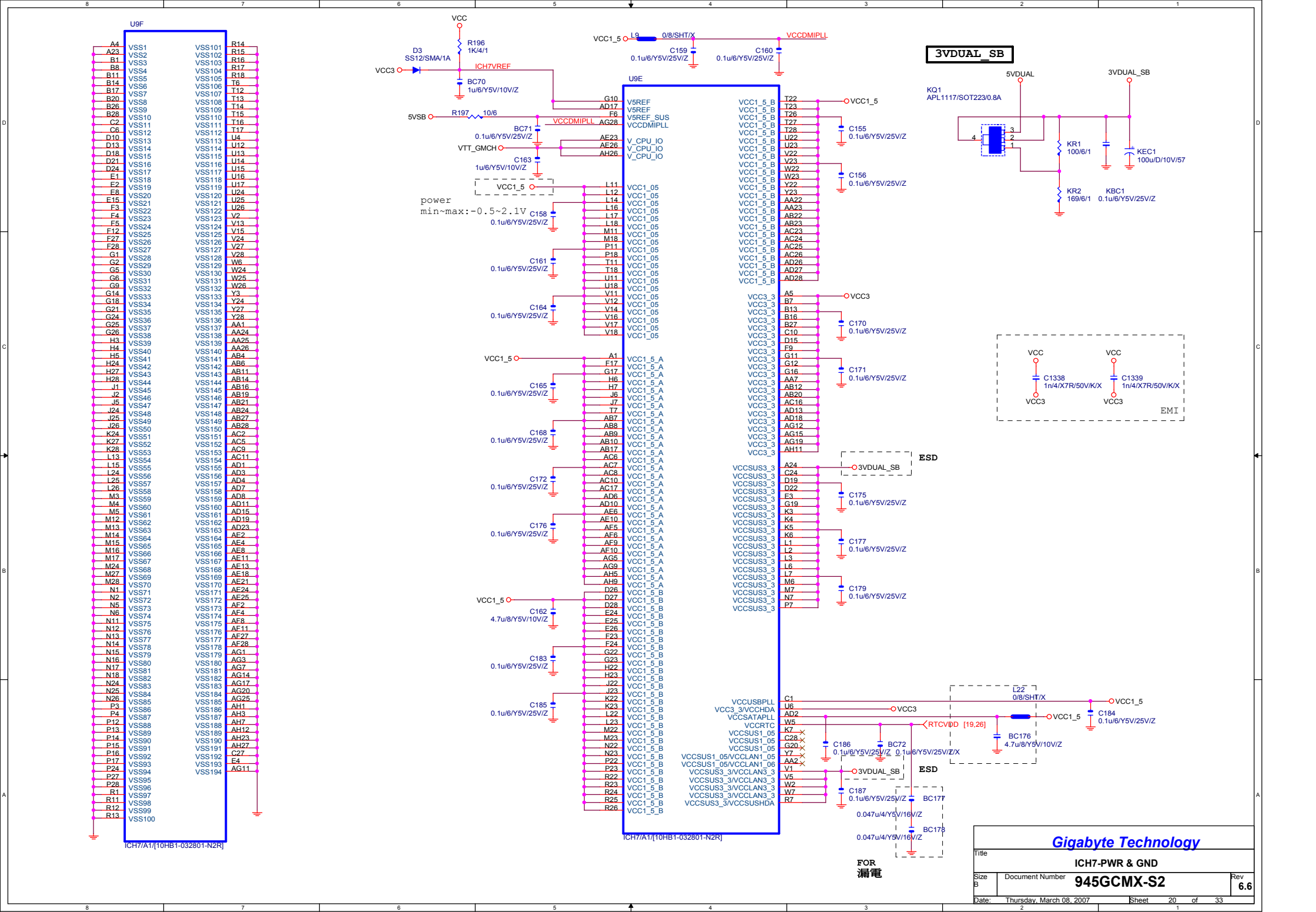
EXP A TXP0	C92	0.1u4Y5V/16V/Z	EXP A TXP0C
EXP A TXN0	C93	0.1u4Y5V/16V/Z	EXP A TXN0C
EXP A TXP1	C94	0.1u4Y5V/16V/Z	EXP A TXP1C
EXP A TXN1	C95	0.1u4Y5V/16V/Z	EXP A TXN1C
EXP A TXP2	C96	0.1u4Y5V/16V/Z	EXP A TXP2C
EXP A TXN2	C97	0.1u4Y5V/16V/Z	EXP A TXN2C
EXP A TXP3	C98	0.1u4Y5V/16V/Z	EXP A TXP3C
EXP A TXN3	C99	0.1u4Y5V/16V/Z	EXP A TXN3C
EXP A TXP4	C100	0.1u4Y5V/16V/Z	EXP A TXP4C
EXP A TXN4	C101	0.1u4Y5V/16V/Z	EXP A TXN4C
EXP A TXP5	C102	0.1u4Y5V/16V/Z	EXP A TXP5C
EXP A TXN5	C103	0.1u4Y5V/16V/Z	EXP A TXN5C
EXP A TXP6	C104	0.1u4Y5V/16V/Z	EXP A TXP6C
EXP A TXN6	C105	0.1u4Y5V/16V/Z	EXP A TXN6C
EXP A TXP7	C106	0.1u4Y5V/16V/Z	EXP A TXP7C
EXP A TXN7	C107	0.1u4Y5V/16V/Z	EXP A TXN7C
EXP A TXP8	C108	0.1u4Y5V/16V/Z	EXP A TXP8C
EXP A TXN8	C109	0.1u4Y5V/16V/Z	EXP A TXN8C
EXP A TXP9	C110	0.1u4Y5V/16V/Z	EXP A TXP9C
EXP A TXN9	C111	0.1u4Y5V/16V/Z	EXP A TXN9C
EXP A TXP10	C112	0.1u4Y5V/16V/Z	EXP A TXP10C
EXP A TXN10	C113	0.1u4Y5V/16V/Z	EXP A TXN10C
EXP A TXP11	C114	0.1u4Y5V/16V/Z	EXP A TXP11C
EXP A TXN11	C115	0.1u4Y5V/16V/Z	EXP A TXN11C
EXP A TXP12	C116	0.1u4Y5V/16V/Z	EXP A TXP12C
EXP A TXN12	C117	0.1u4Y5V/16V/Z	EXP A TXN12C
EXP A TXP13	C118	0.1u4Y5V/16V/Z	EXP A TXP13C
EXP A TXN13	C119	0.1u4Y5V/16V/Z	EXP A TXN13C
EXP A TXP14	C120	0.1u4Y5V/16V/Z	EXP A TXP14C
EXP A TXN14	C121	0.1u4Y5V/16V/Z	EXP A TXN14C
EXP A TXP15	C122	0.1u4Y5V/16V/Z	EXP A TXP15C
EXP A TXN15	C123	0.1u4Y5V/16V/Z	EXP A TXN15C

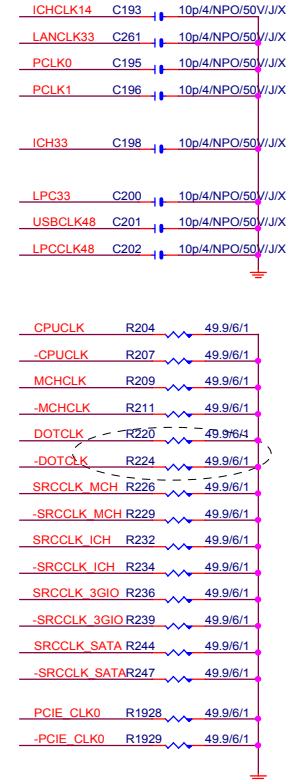
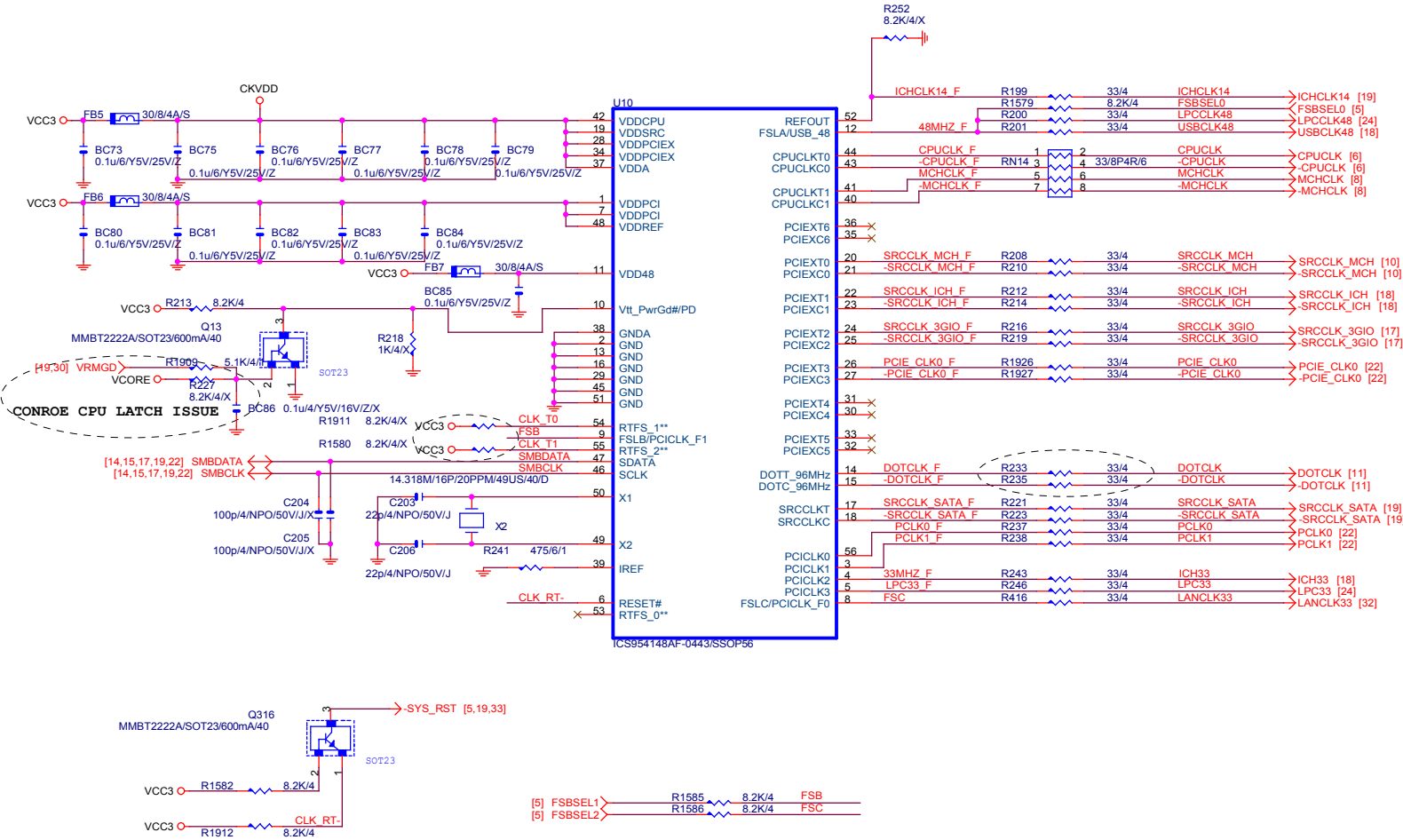
EXP A RXP0	EXP A RXN0C
EXP A RXP1	EXP A RXN1C
EXP A RXN1	EXP A RXP1C
EXP A RXP2	EXP A RXN2C
EXP A RXN2	EXP A RXP2C
EXP A RXP3	EXP A RXN3C
EXP A RXN3	EXP A RXP3C
EXP A RXP4	EXP A RXN4C
EXP A RXN4	EXP A RXP4C
EXP A RXP5	EXP A RXN5C
EXP A RXN5	EXP A RXP5C
EXP A RXP6	EXP A RXN6C
EXP A RXN6	EXP A RXP6C
EXP A RXP7	EXP A RXN7C
EXP A RXN7	EXP A RXP7C
EXP A RXP8	EXP A RXN8C
EXP A RXN8	EXP A RXP8C
EXP A RXP9	EXP A RXN9C
EXP A RXN9	EXP A RXP9C
EXP A RXP10	EXP A RXN10C
EXP A RXN10	EXP A RXP10C
EXP A RXP11	EXP A RXN11C
EXP A RXN11	EXP A RXP11C
EXP A RXP12	EXP A RXN12C
EXP A RXN12	EXP A RXP12C
EXP A RXP13	EXP A RXN13C
EXP A RXN13	EXP A RXP13C
EXP A RXP14	EXP A RXN14C
EXP A RXN14	EXP A RXP14C
EXP A RXP15	EXP A RXN15C
EXP A RXN15	EXP A RXP15C



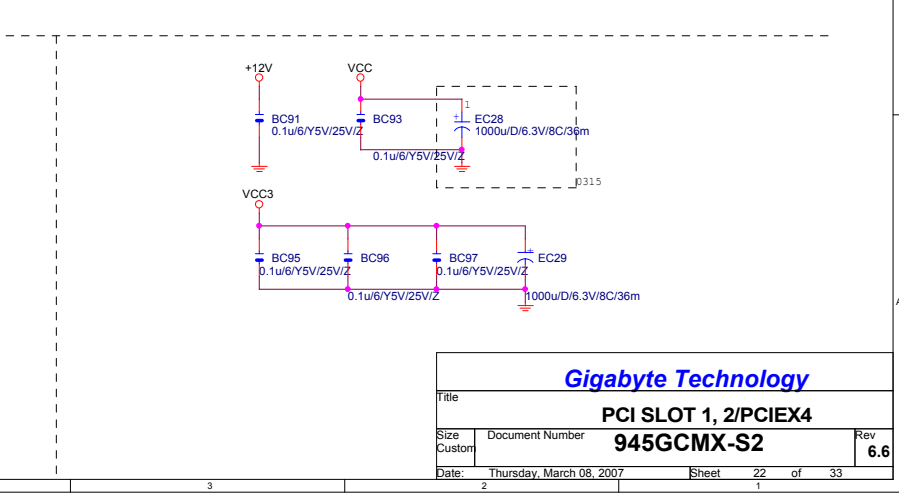
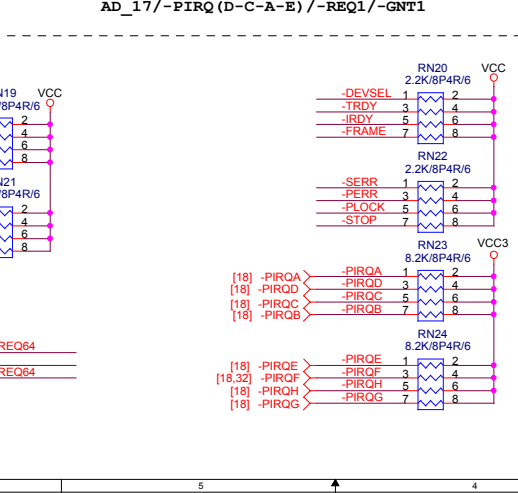
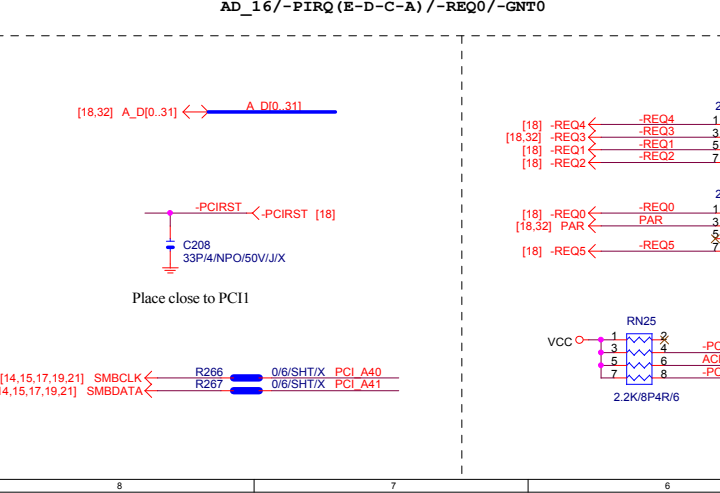
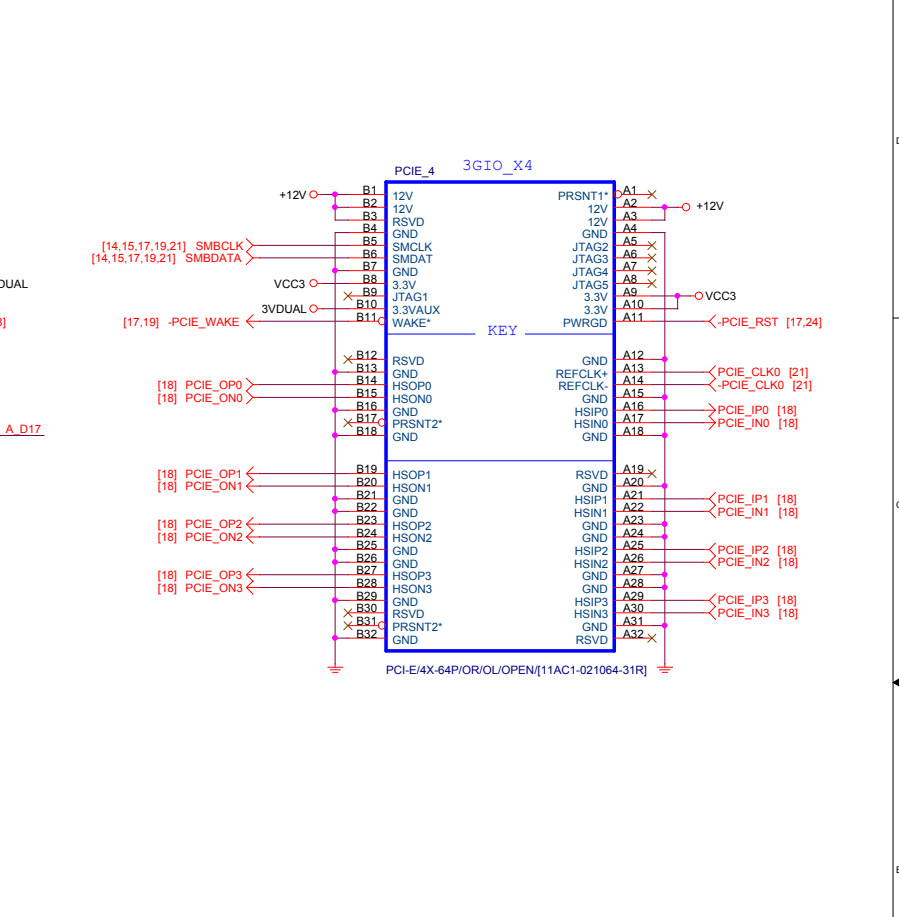
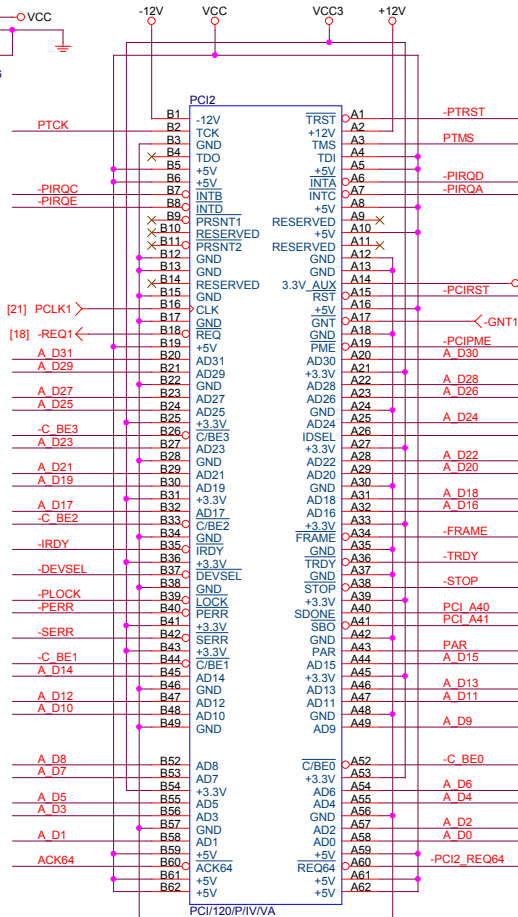
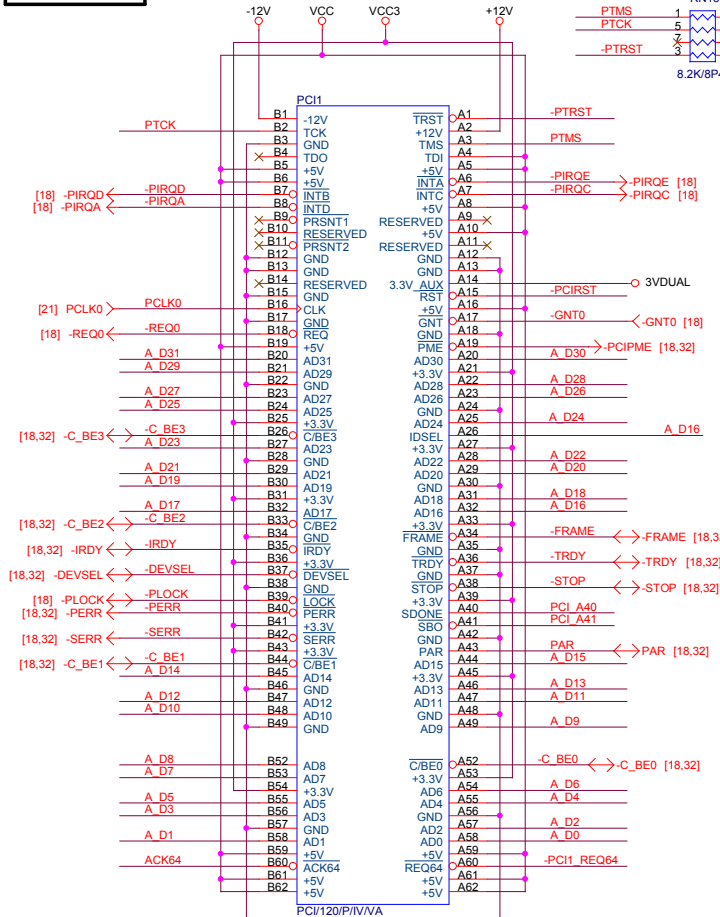






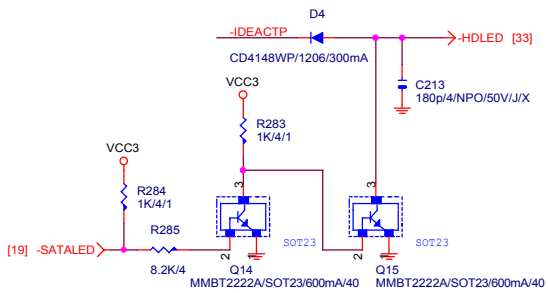


PCI1, 2 SLOT

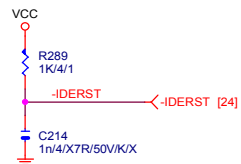


Gigabyte Technology			
PCI SLOT 1, 2/PCIEX4			
945GCMX-S2			
Rev 6.6			
Title	Document Number	2	Sheet 22 of 33
Size	Custom	Thursday, March 08, 2007	

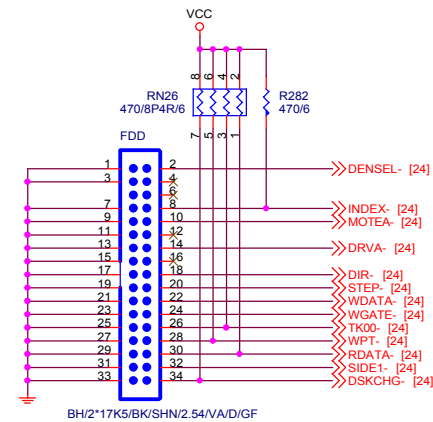
IDE/SATA LED



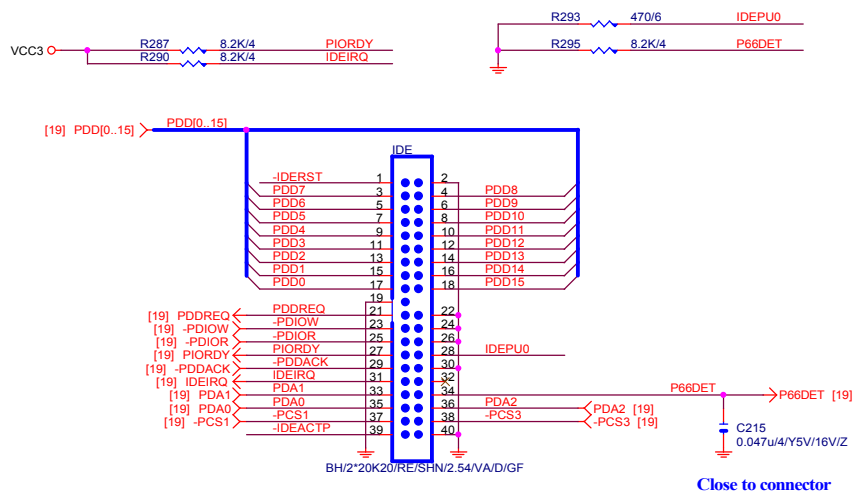
IDE RESET



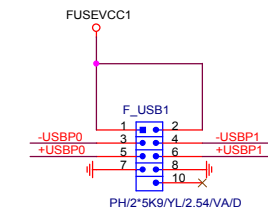
FLOPPY



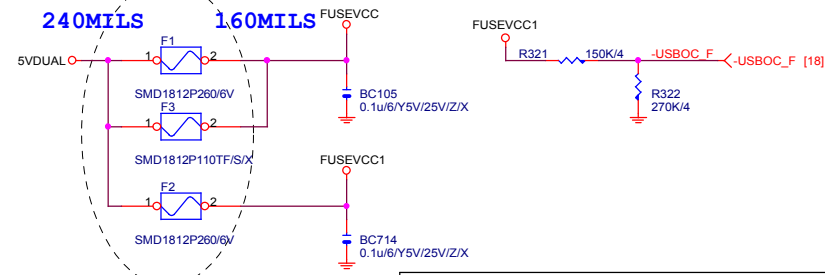
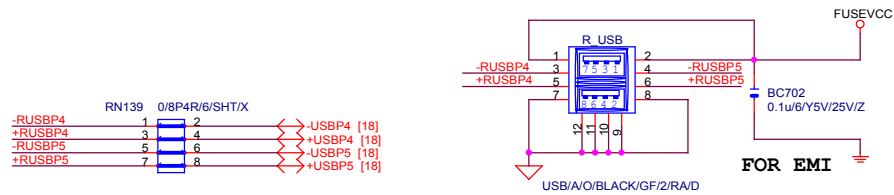
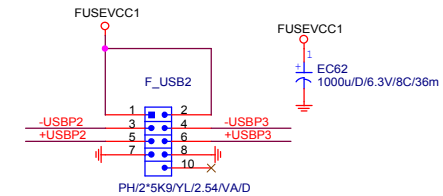
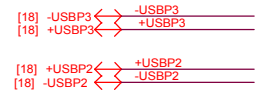
IDE



FRONT USB1



FRONT USB2

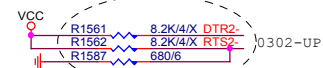


Gigabyte Technology

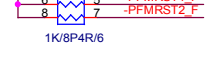
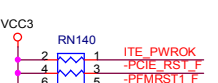
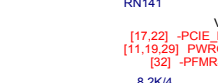
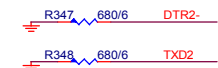
Title		
IDE,FDD,F_USB		
Size	Document Number	Rev
B	945GCMX-S2	6.6
Date:	Thursday, March 08, 2007	Sheet 23 of 33

```
RTS2- ==LOW CPU FAN 50%
```

DEFAULT 50%



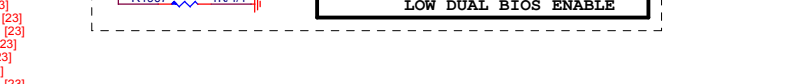
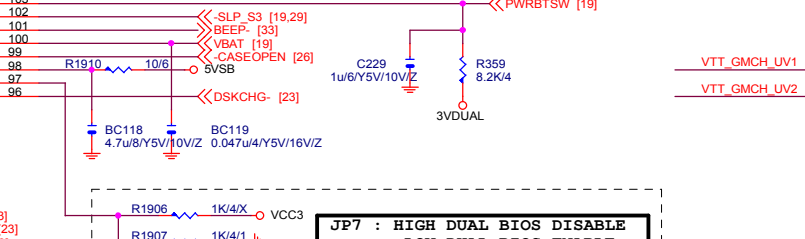
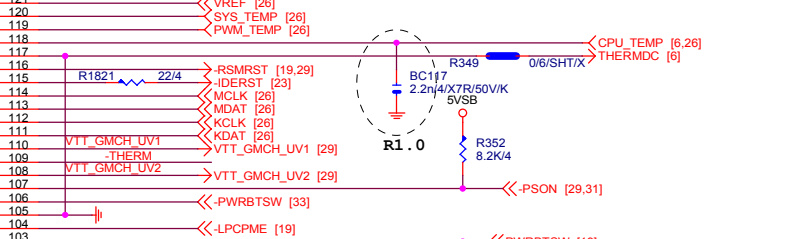
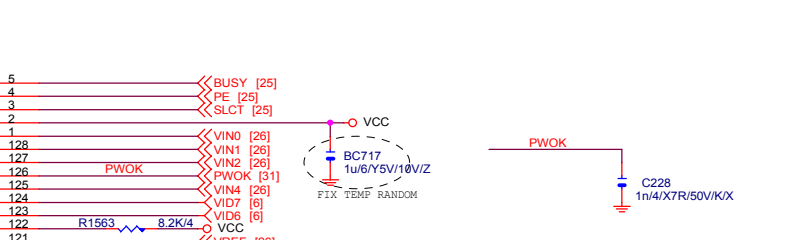
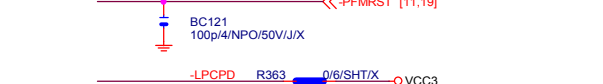
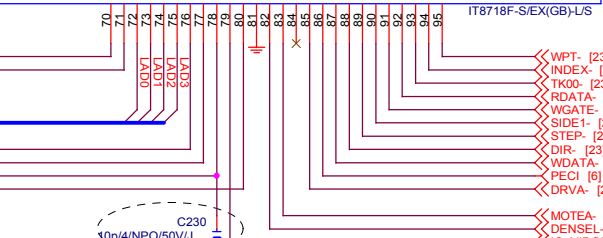
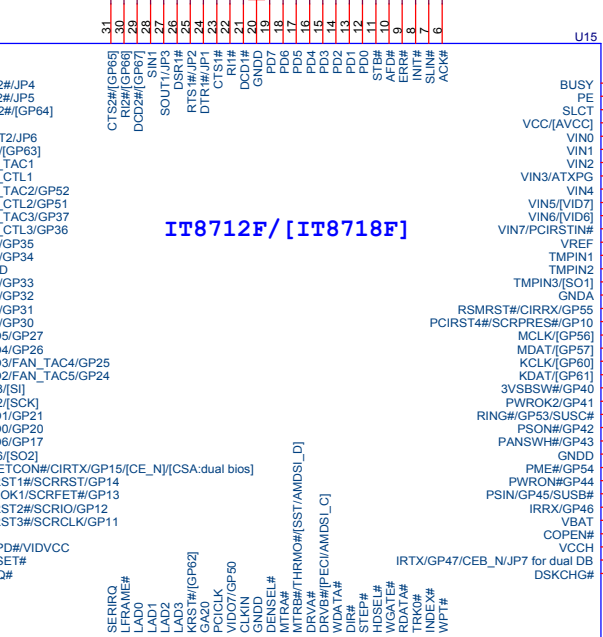
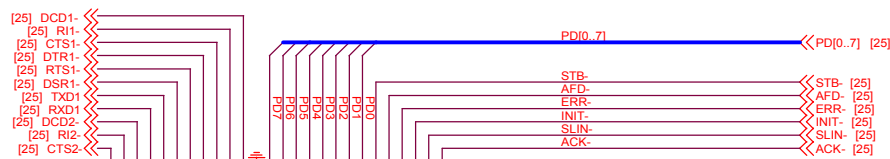
SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V



Dual BIOS:
GB logo :Pin 61 (GP15/CSA)

Pin 59 Dual BIOS ,Power On Strapping:
H ==>Dual BIOS function Enable
L ==>Dual BIOS function Disable

1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接 3.3V
LPCPD#=VIDVCC



JP7 : HIGH DUAL BIOS DISABLE
LOW DUAL BIOS ENABLE

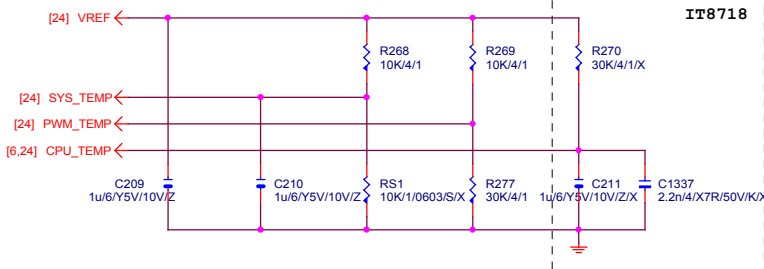
Gigabyte Technology

ITE 8718 LPC IO

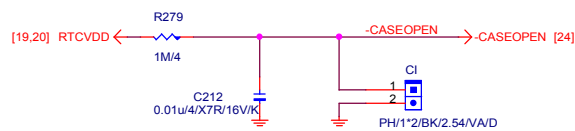
Size B	Document Number 945GCMX-S2
-----------	--------------------------------------

Date:	Thursday, March 08, 2007	Sheet	24	of	33
-------	--------------------------	-------	----	----	----

TEMP H/W MONITOR

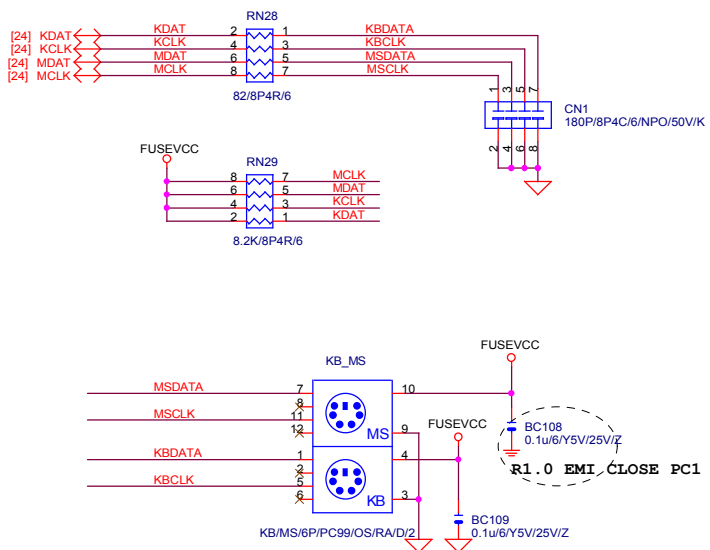


CASE OPEN

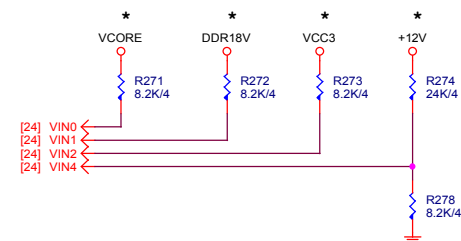


Case Open Circuits

KB/MS



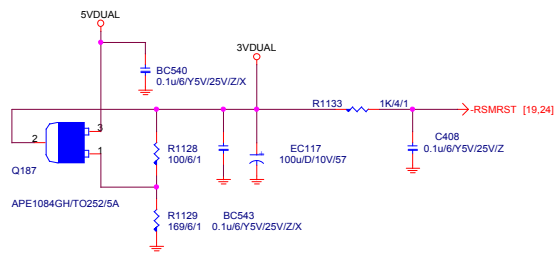
VOLTAGE-- H/W MONITOR



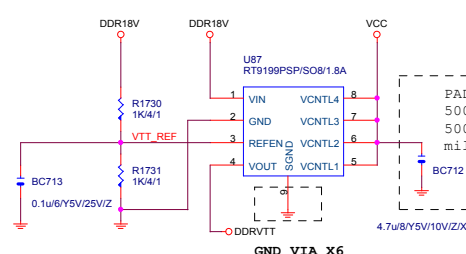
Gigabyte Technology

Title		
BIOS/HW-MONITOR/CI/KB/MS		
Size B	Document Number	Rev
	945GCMX-S2	6.6
Date:	Thursday, March 08, 2007	Sheet 26 of 33

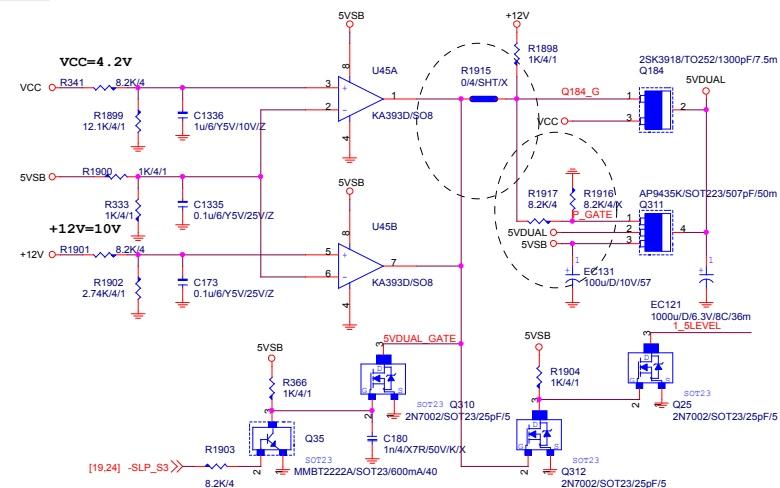
3VDUAL CIRCUIT



DDRVTT

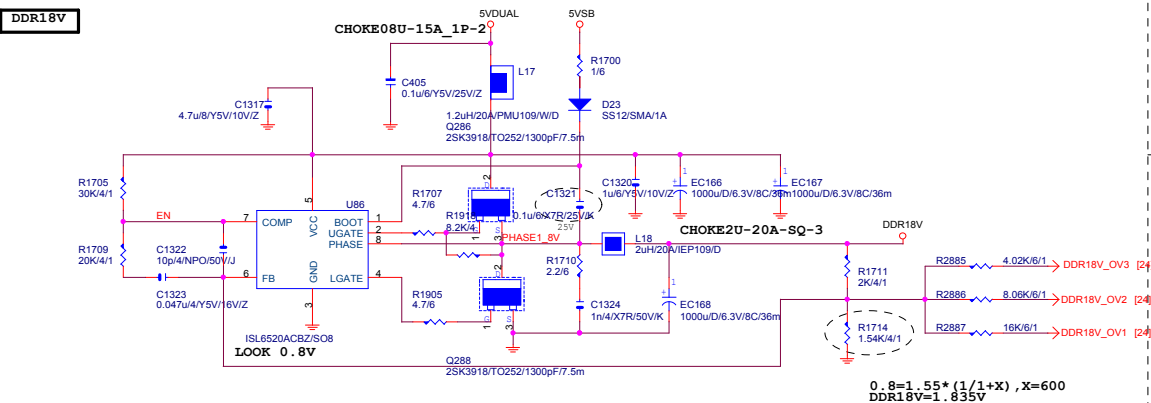


5VDUAL

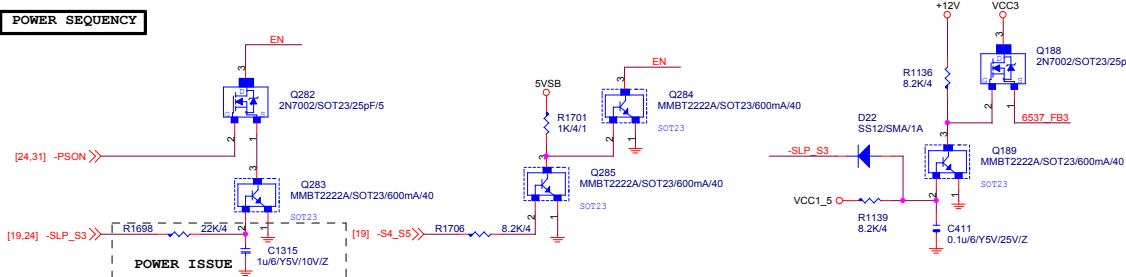


S3 TURN OFF 2.5LEVEL, 避免DDR18V DROP
(因PSU +12V太晚關, 造成OF TURN
ON, 導致DDR18V LOADING WORSE)

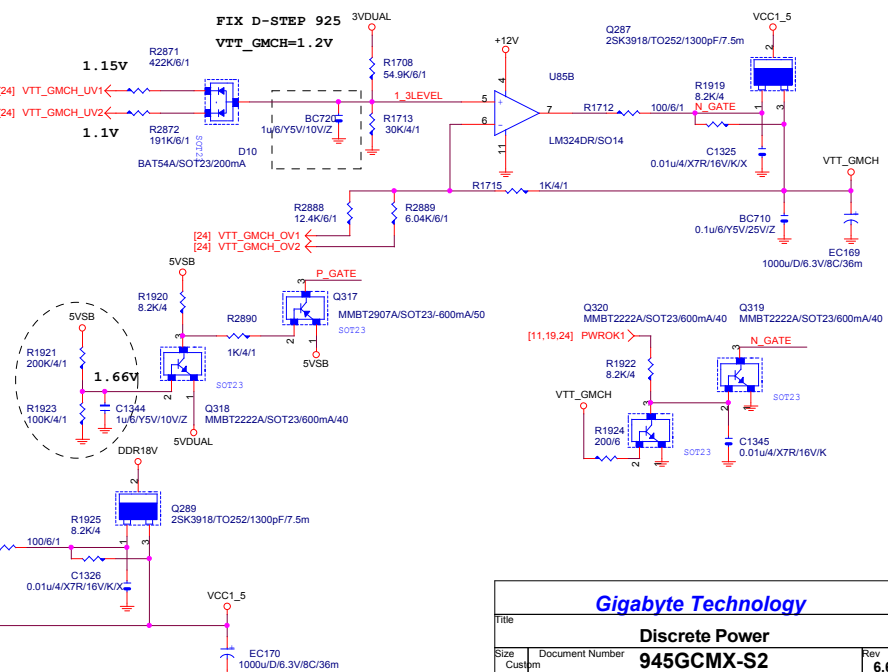
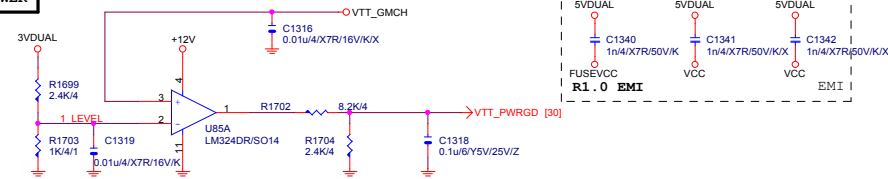
DDR18V



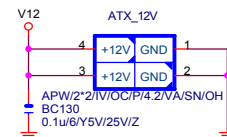
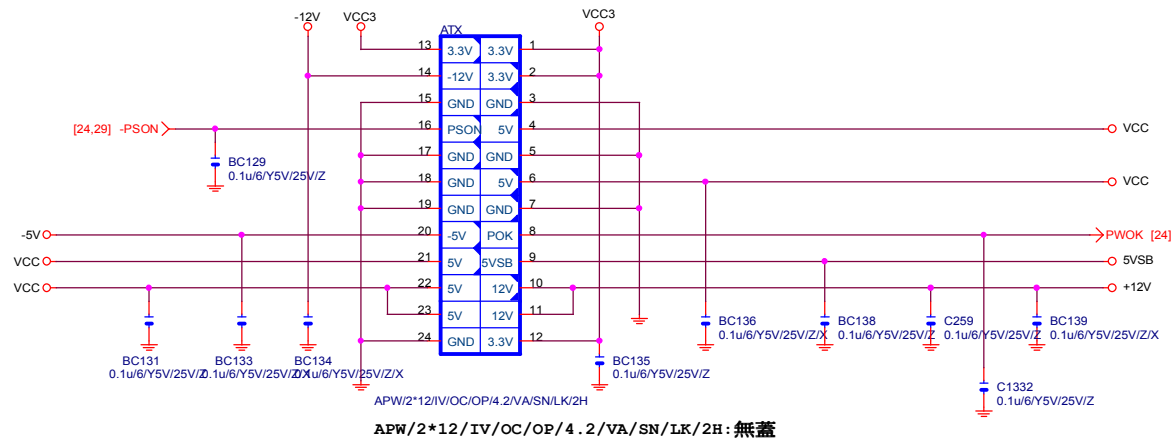
POWER SEQUENCY



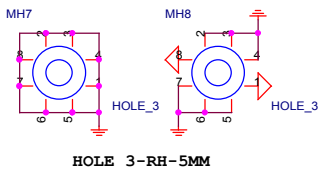
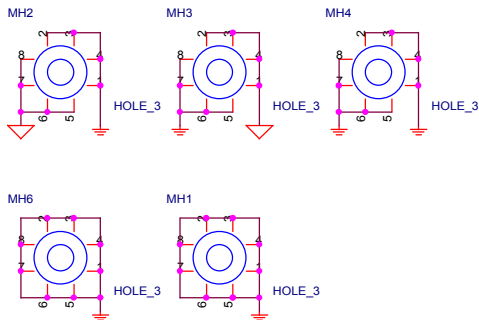
POWER



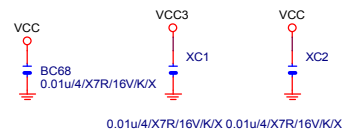
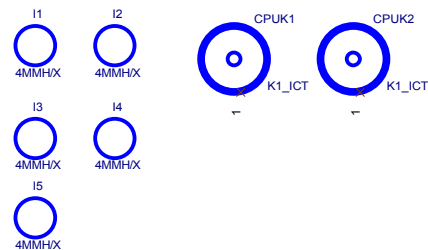
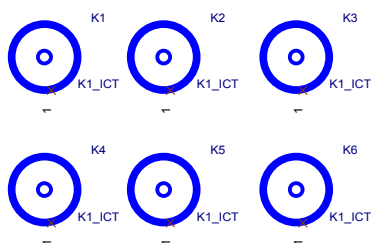
ATXPWR_24-2 ATX POWER CONNECTOR

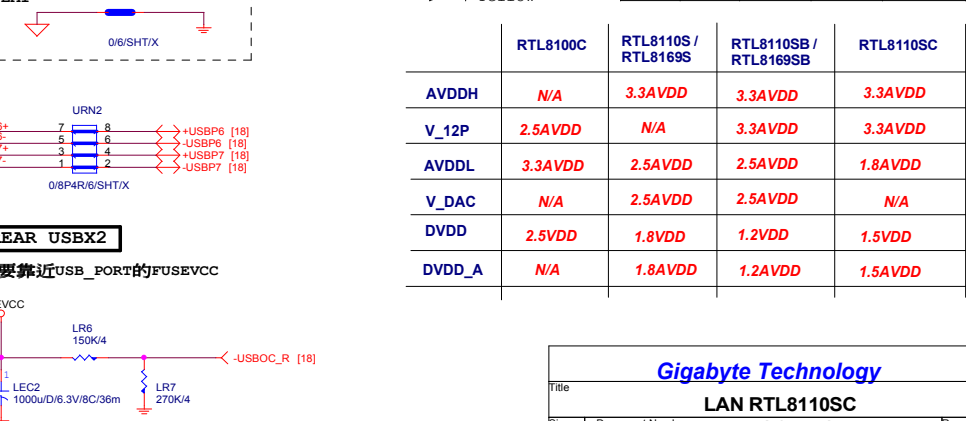
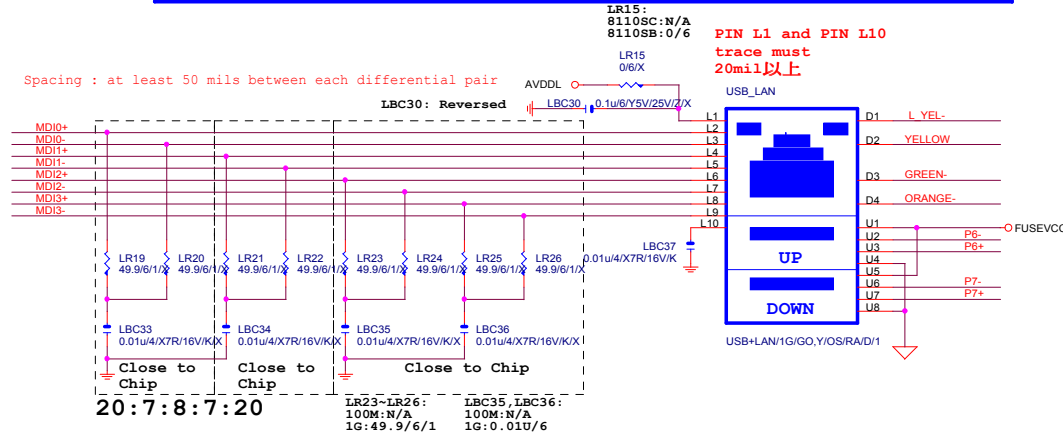


HOLE_3-RH-2

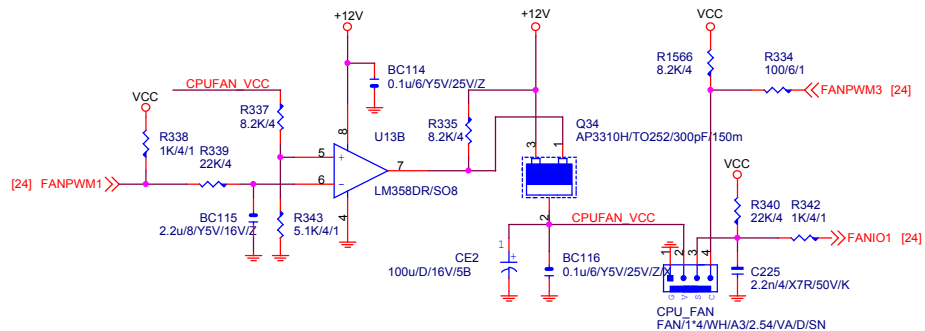


HOLE_3-RH-5MM

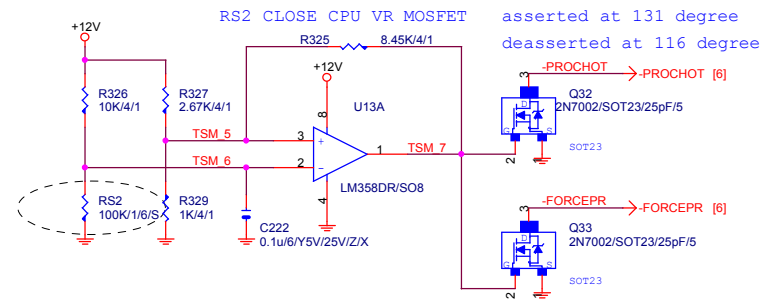




CPU SMART FAN SMART FAN

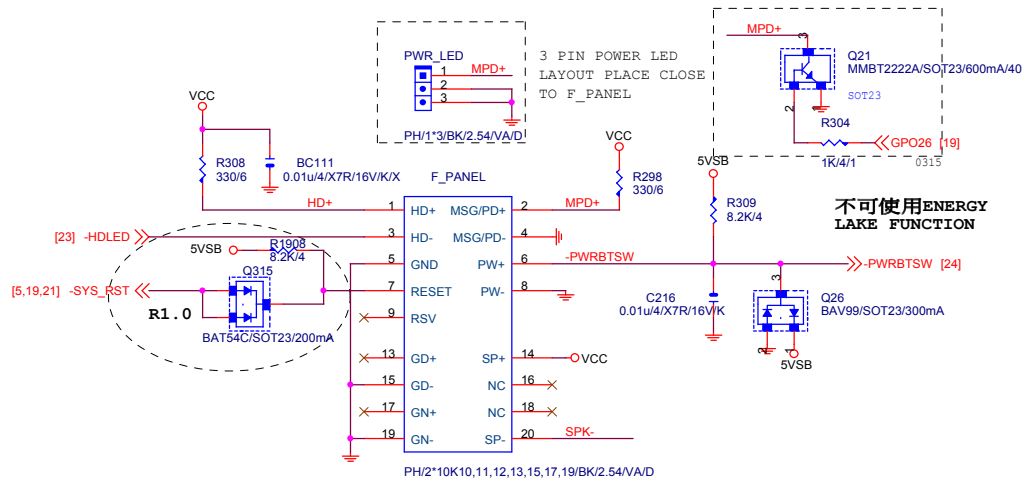


PROCESSOR HOT

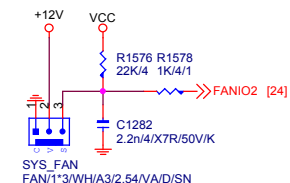


INTEL FRONT PANEL

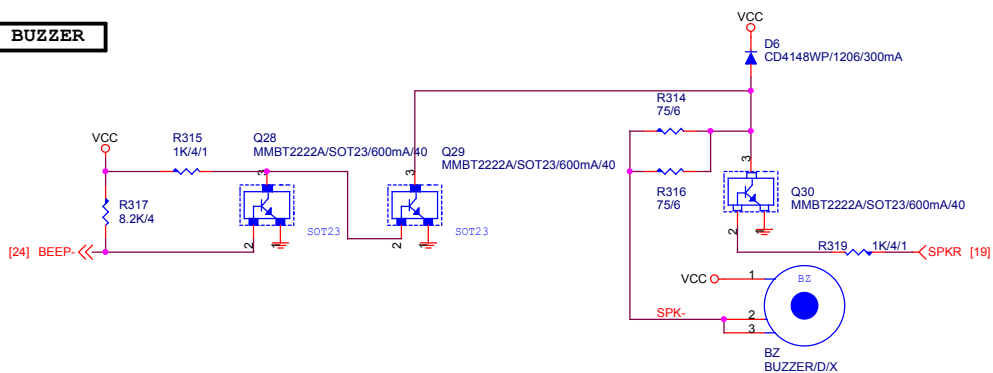
MPD- : (GPIO25--VCCSUS3+HI+HI+DEFINED (C3/C4/S/1/S3/S/4/S5)) -->INTEL



SYS_FAN



BUZZER



Gigabyte Technology			
Title			
FRONT PANEL			
Size	Document Number	Rev	
Custom	945GCMX-S2	6.6	
Date:	Thursday, March 08, 2007	Sheet	33 of 33